

# Compal confidential

## Schematics Document

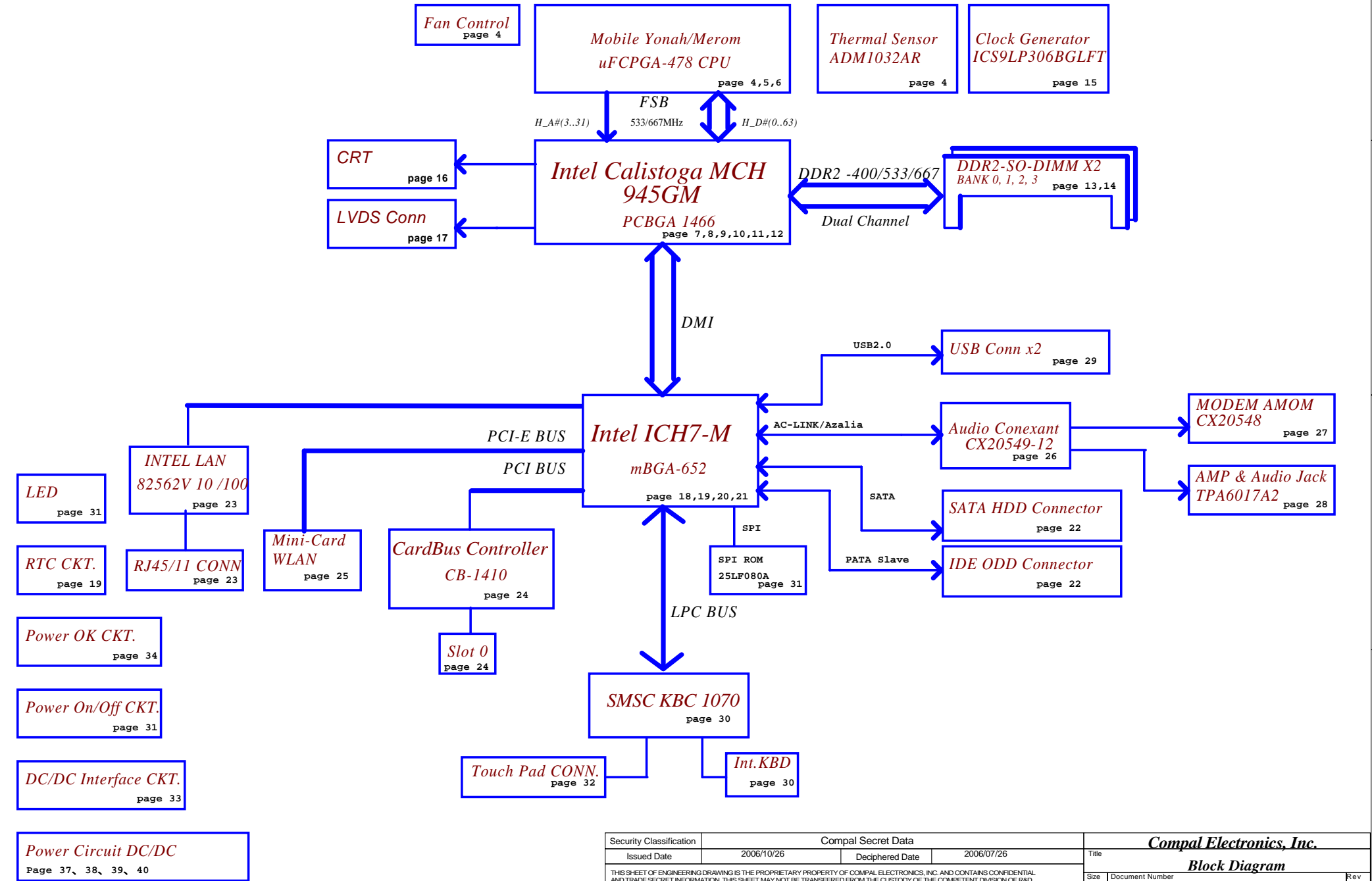
### Mobile Yonah uFCPGA with Intel Calistoga\_GM+ ICH7-M core logic

2006-12-11

REV:0.1

Security Classification	Compal Secret Data			Title	
Issued Date	2006/10/26	Deciphered Date	2006/07/26	Cover Sheet	
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# Volga 2.0



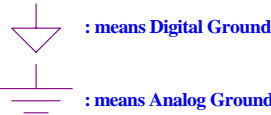
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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (18.5V)	NA	NA	NA
B+	AC or battery power rail for power circuit	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V power rail for Processor I/O and MCH/ICH core power	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDRII Vtt	ON	OFF	OFF
+1.5VS	1.5V switched power rail for PCI-E interface	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail for MCH video PLL	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_VCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

Symbol Note :



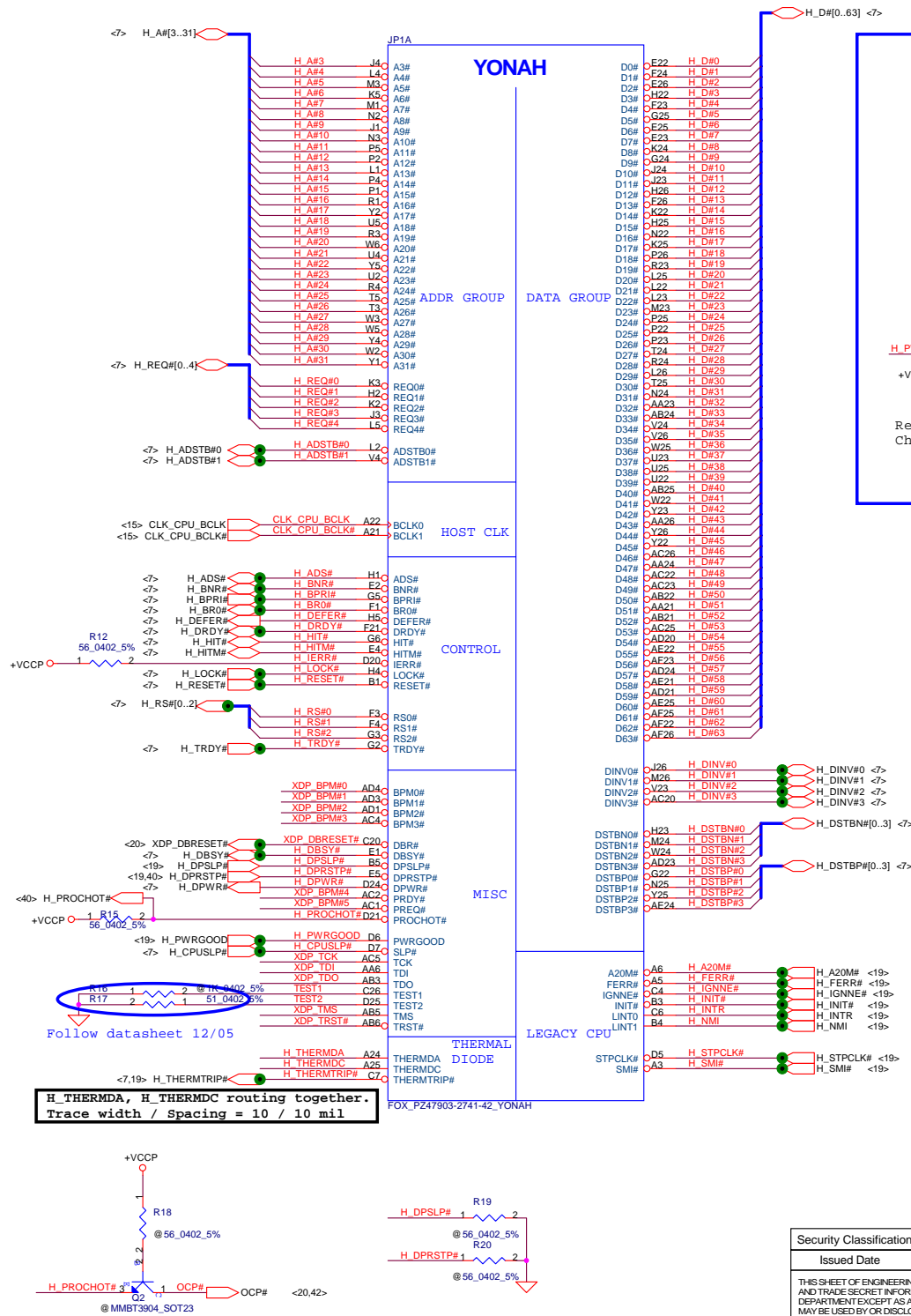
- @ : means just reserve , no build
- UMA @ : means build UMA sku with Intel 945GM .
- SPI@ : means just build when SPI I/F BIOS function reserve.
- NOXDP@ : means just build when XDP function disable.
- XDP@ : means just build when XDP function enable. When this time, docking PCI express will not work.
- LP@ : means just build when Low power clock gen. install
- NOLP@ : means just build when Low power clock gen. NO install
- 45@ : means need be mounted when 45 level assy or rework stage.
- FWH@ : means just build when FWH I/F BIOS function reserve.

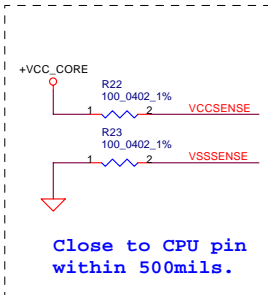
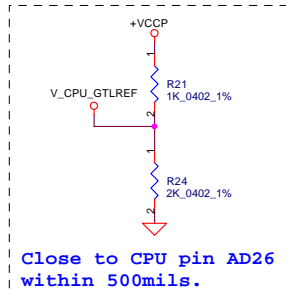
External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
CARD BUS	D6	AD22	2	C D E G

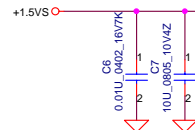
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

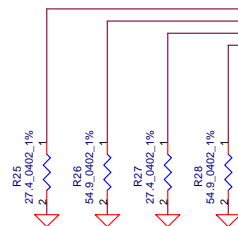




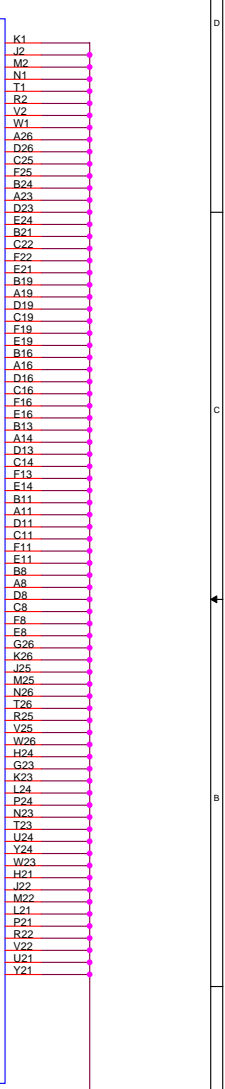
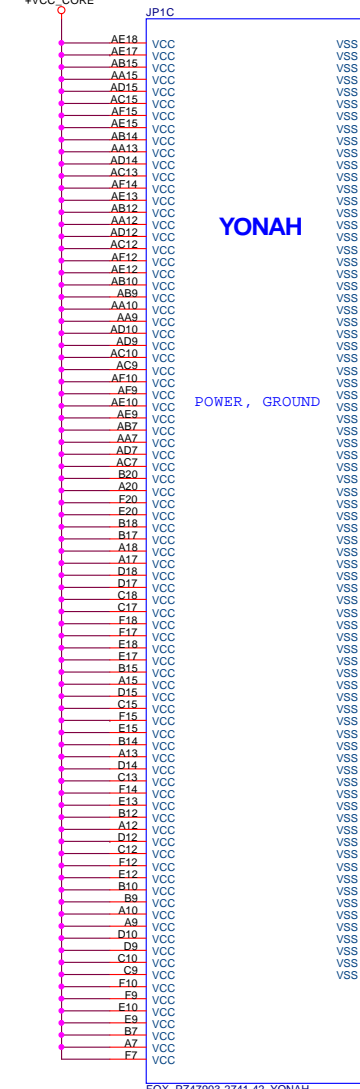
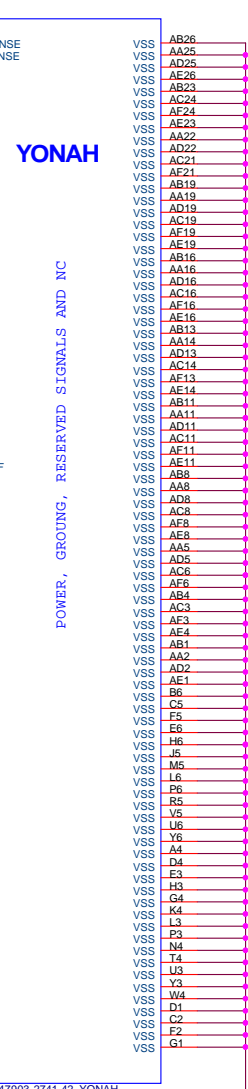
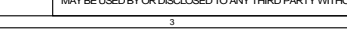
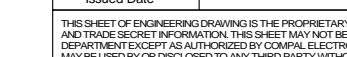
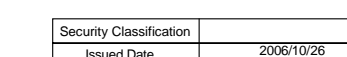
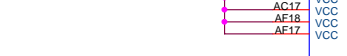
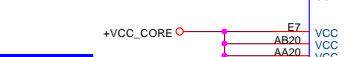
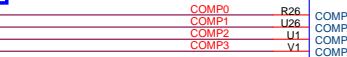
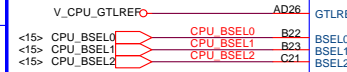
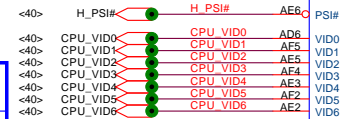
Length match within 25 mils  
The trace width 18 mils space  
7 mils

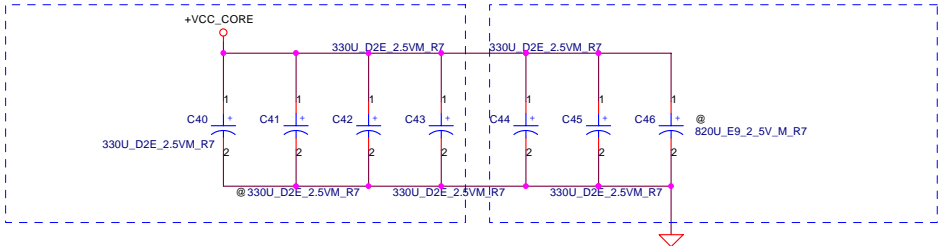
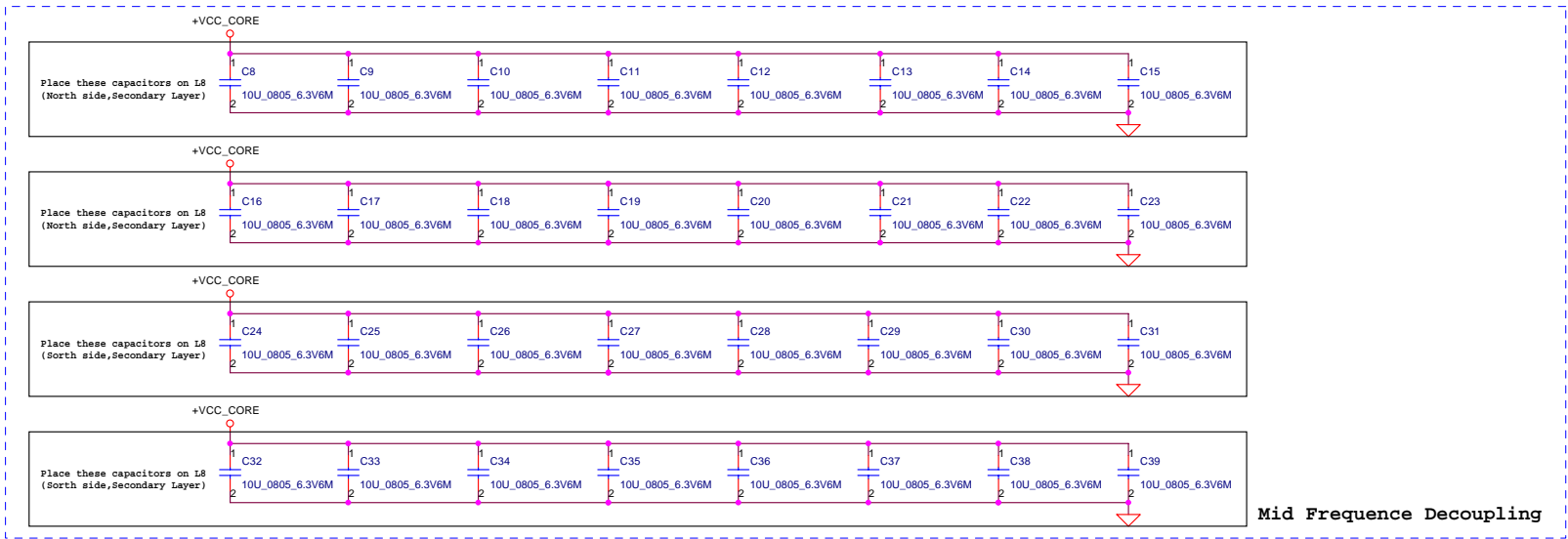


CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

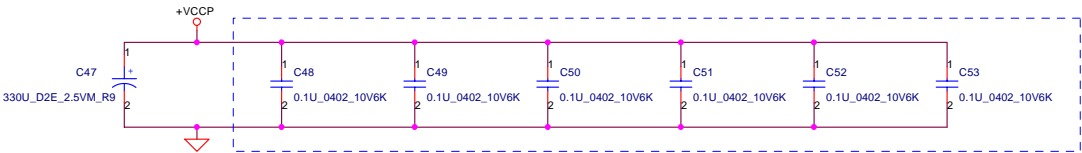


Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.

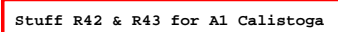
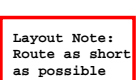




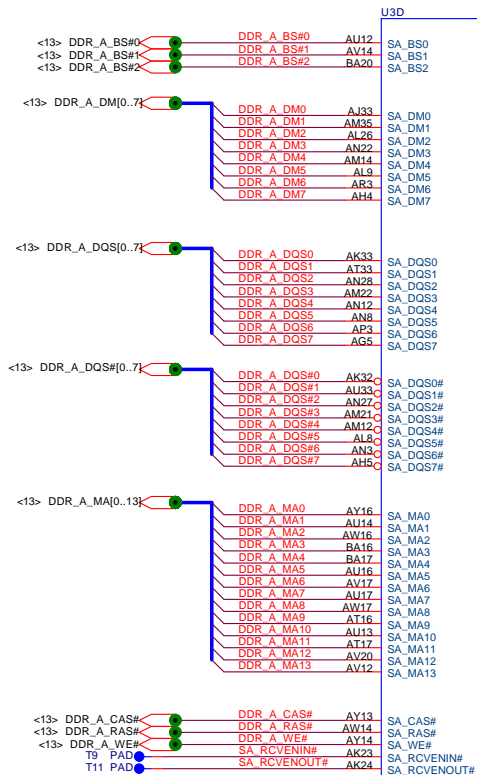
ESR <= 1.5m ohm  
Capacitor > 1980uF



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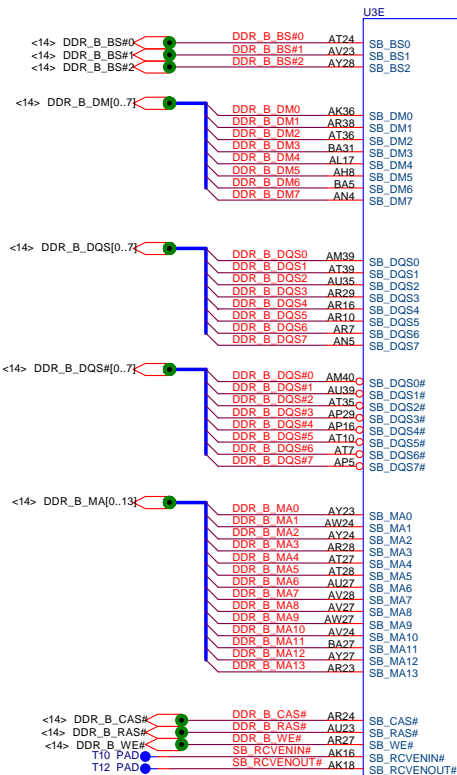
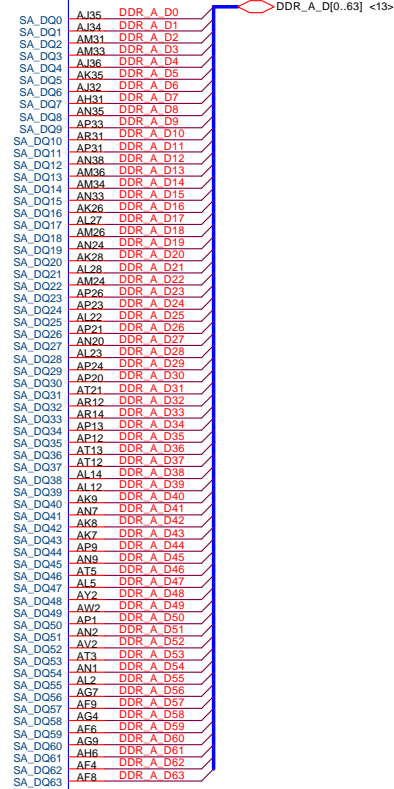


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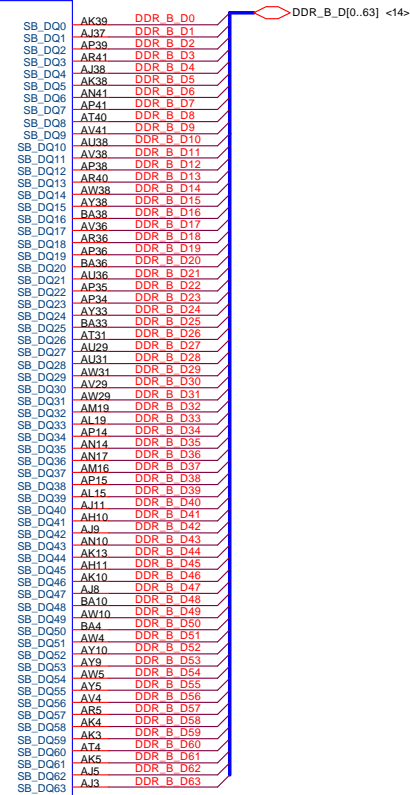
DDR SYS MEMORY A

CALISTOGA\_FCBGA1466-D



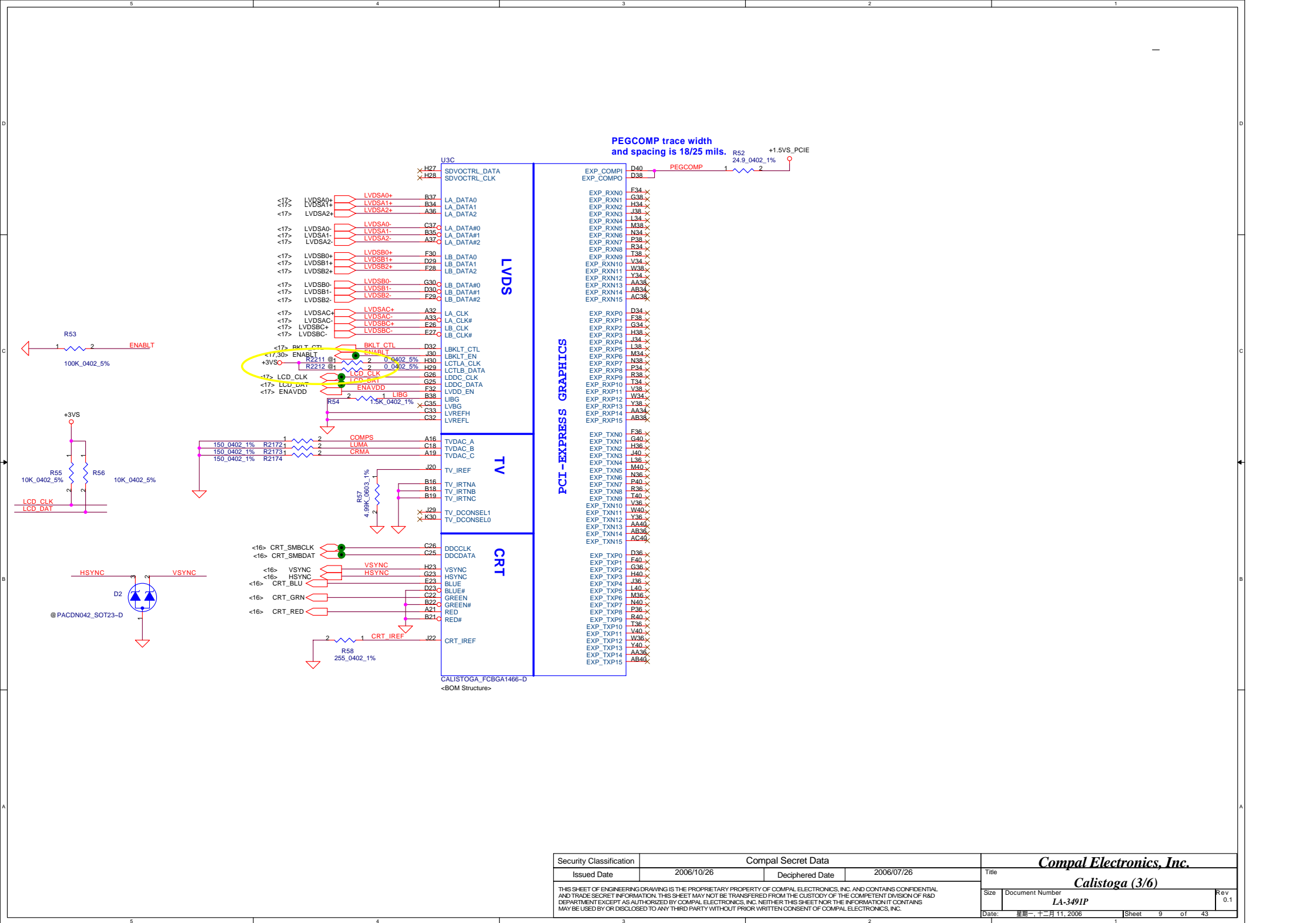
DDR SYS MEMORY B

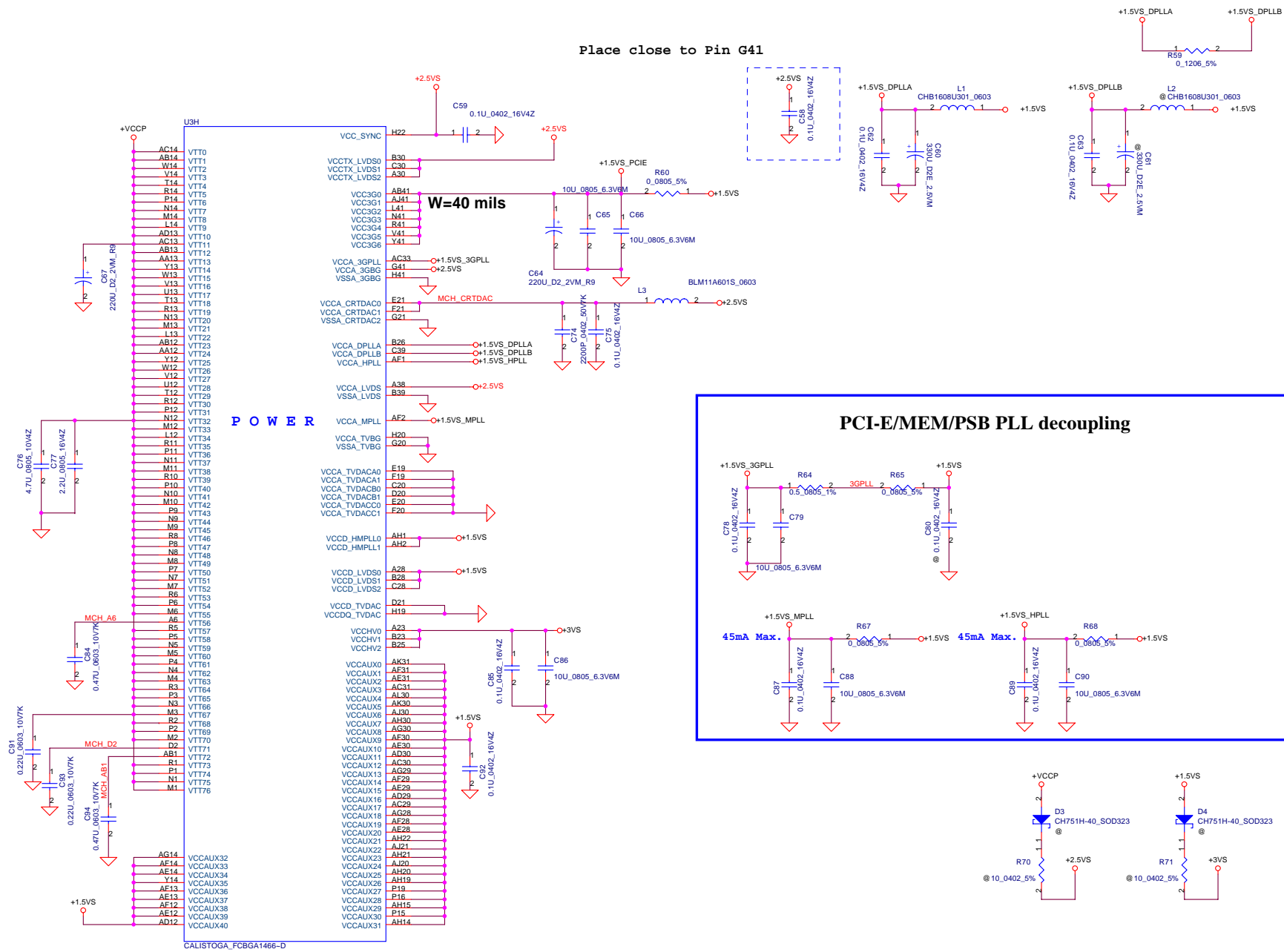
CALISTOGA\_FCBGA1466-D



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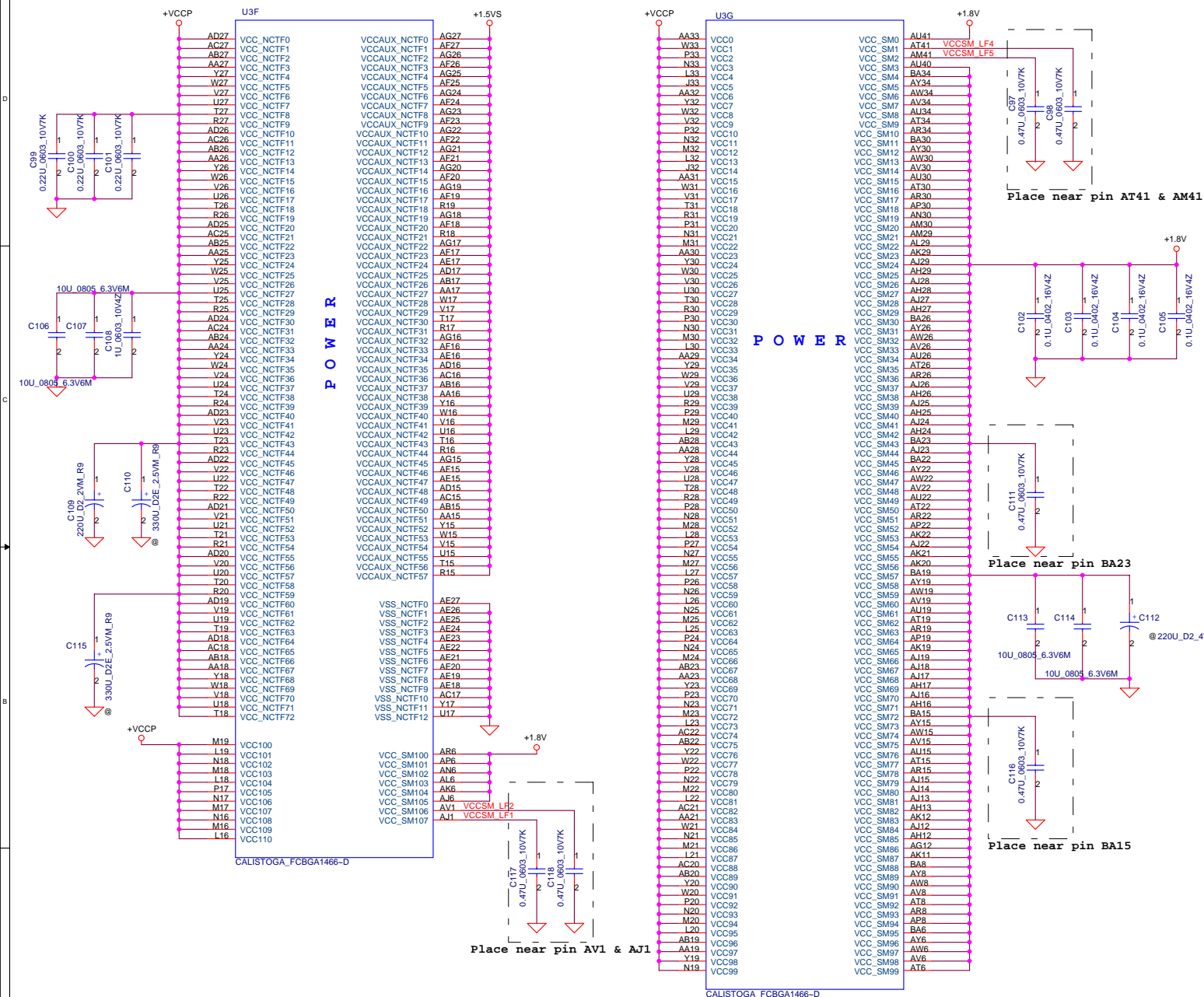
# Strap Pin Table

CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable * 1 = Normal operation (Default)
CFG11	0 = Calistoga * (According to Intel Napa Schematic Checklist & CRB Rev1.301 document 2.2Kohm pull-down resistor) 1 = Reserved
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.05V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.

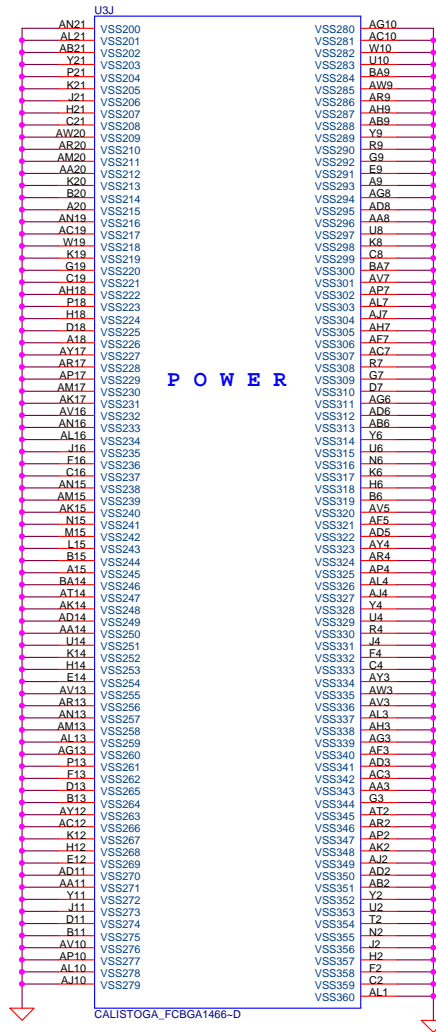
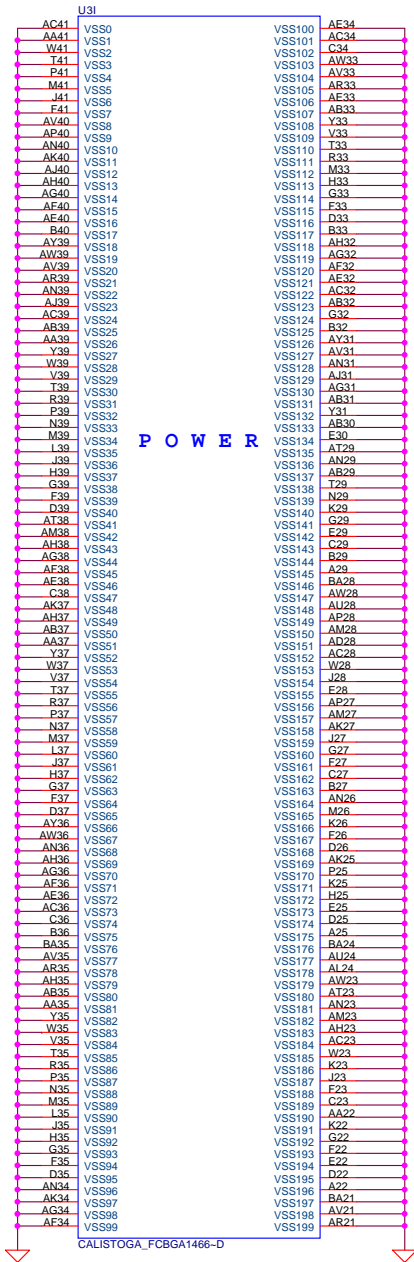
<7>	CFG5	R72	1	2	@ 2.2K 0402 5%
<7>	CFG7	R73	1	2	@ 2.2K 0402 5%
<7>	CFG9	R74	1	2	@ 2.2K 0402 5%
<7>	CFG11	R75	1	2	@ 2.2K 0402 5%
<7>	CFG12	R76	1	2	@ 2.2K 0402 5%
<7>	CFG13	R77	1	2	@ 2.2K 0402 5%
<7>	CFG16	R78	1	2	@ 2.2K 0402 5%
<7>	CFG18	R79	1	2	@ 1K 0402 5%
<7>	CFG19	R80	1	2	@ 1K 0402 5%
<7>	CFG20	R81	1	2	@ 1K 0402 5%



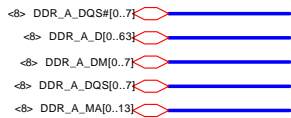
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Calistoga (5/6)

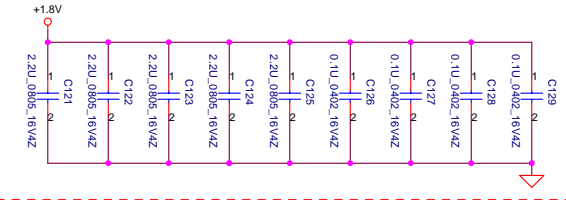
Rev 0.1



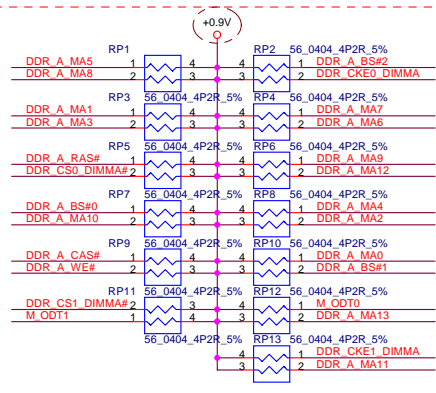
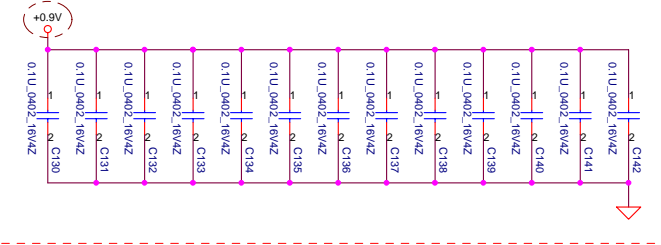
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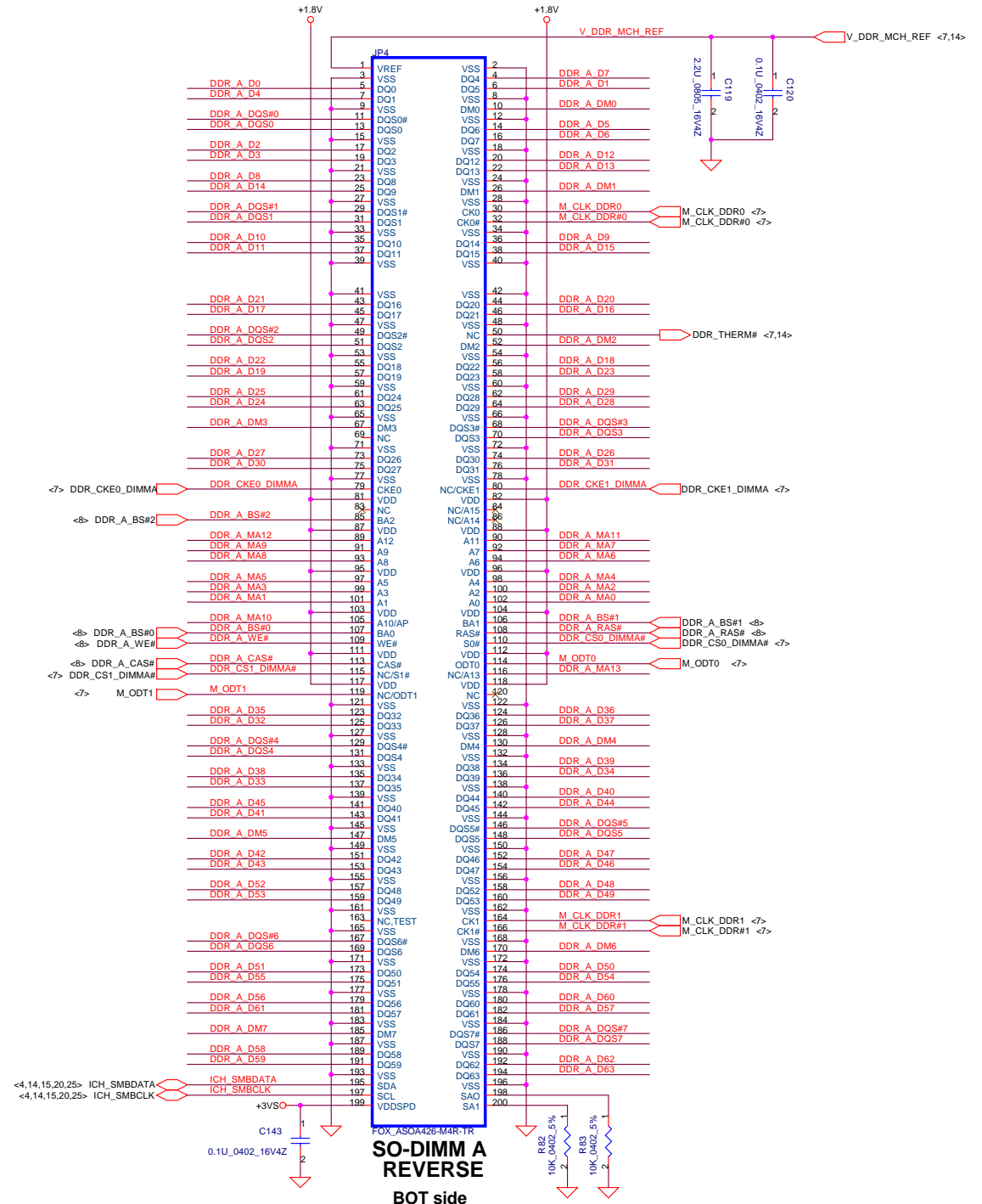
Layout Note:  
Place near JP34



Layout Note:  
Place one cap close to every 2 pullup  
resistors terminated to +0.9V



Layout Note:  
Place these resistor  
closely JP34, all  
trace length Max=1.5"



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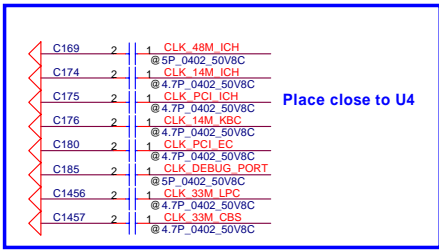
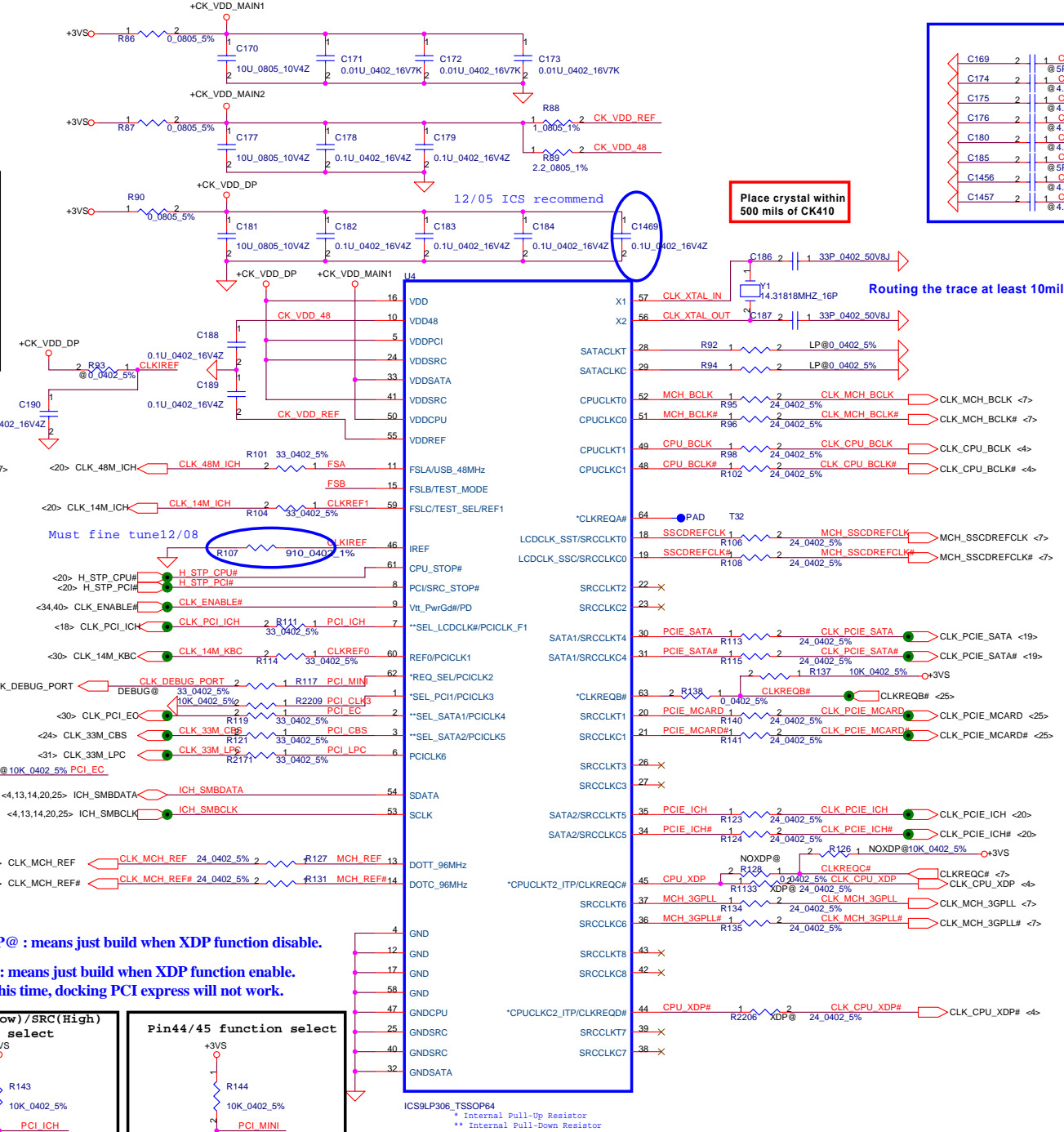
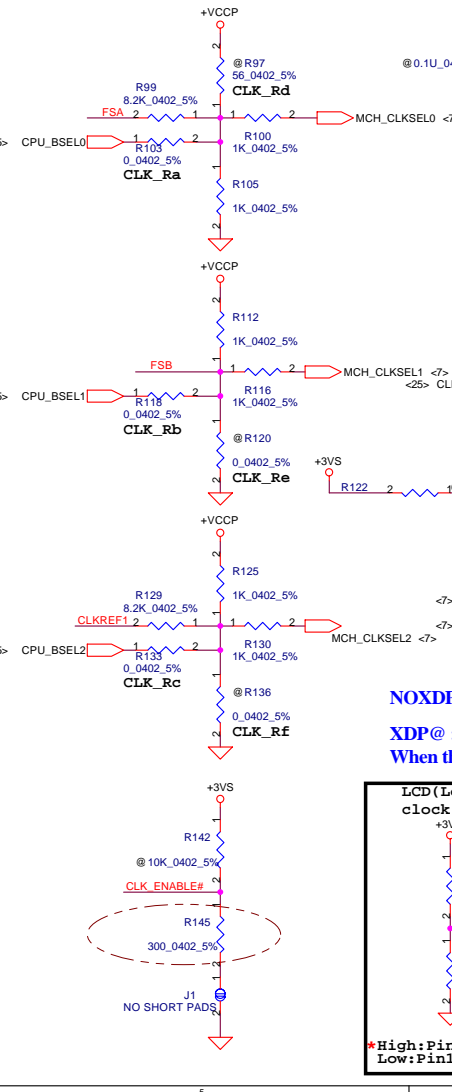


FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS954306

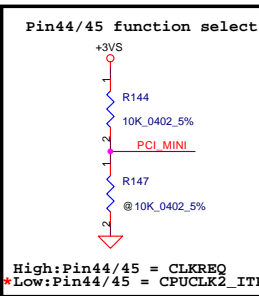
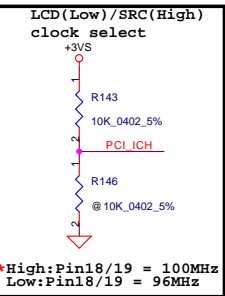
FSB Frequency Set:

CPU Driven	Stuff	CLK_Ra	CLK_Rb	CLK_Rc
* (Default)	No Stuff	CLK_Rd	CLK_Re	CLK_Rf
533MHz	Stuff	CLK_Rd	CLK_Re	CLK_Rf
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc
667MHz	Stuff	CLK_Rd	CLK_Rf	
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc



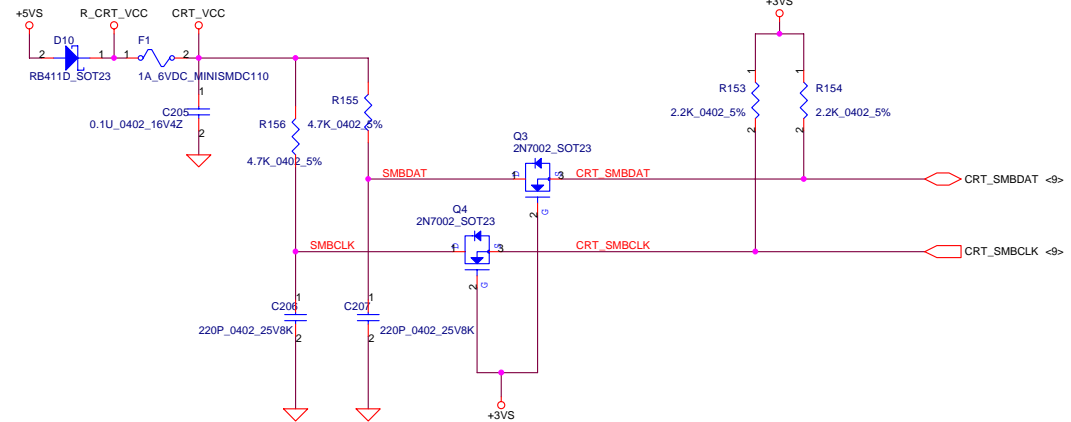
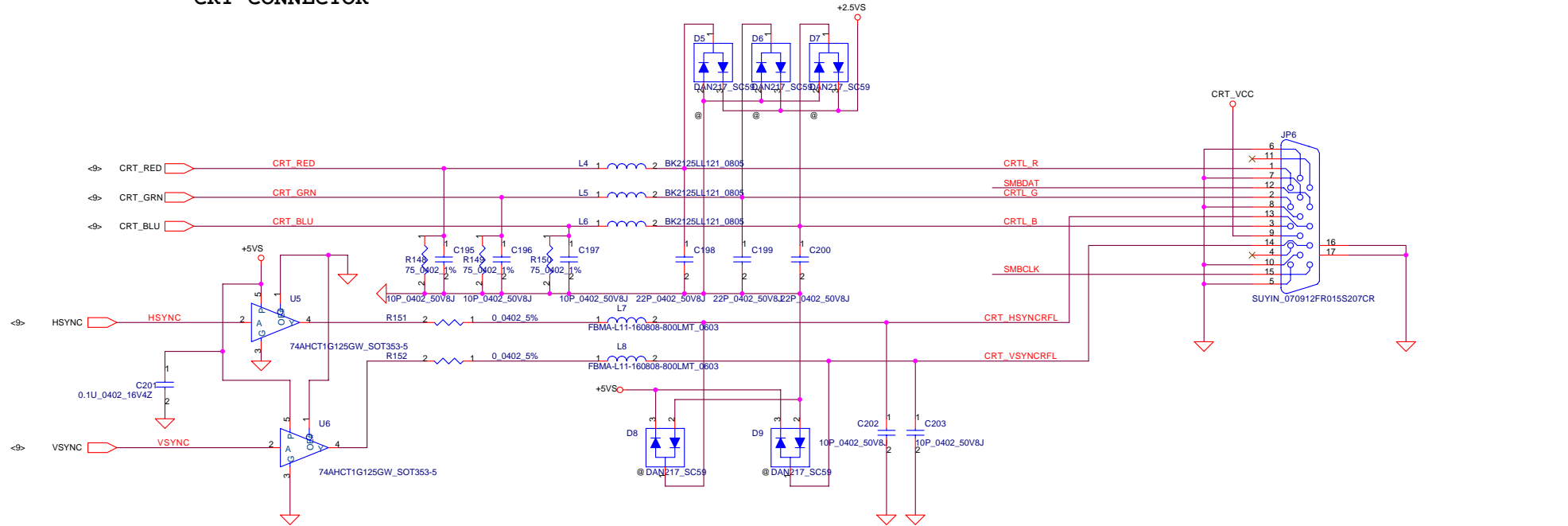
Place near U4  
Place these components  
near each pin within 40  
mils.

NOXDP@ : means just build when XDP function disable.  
XDP@ : means just build when XDP function enable.  
When this time, docking PCI express will not work.



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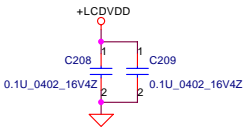
# CRT CONNECTOR



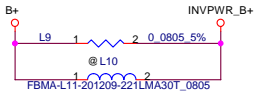
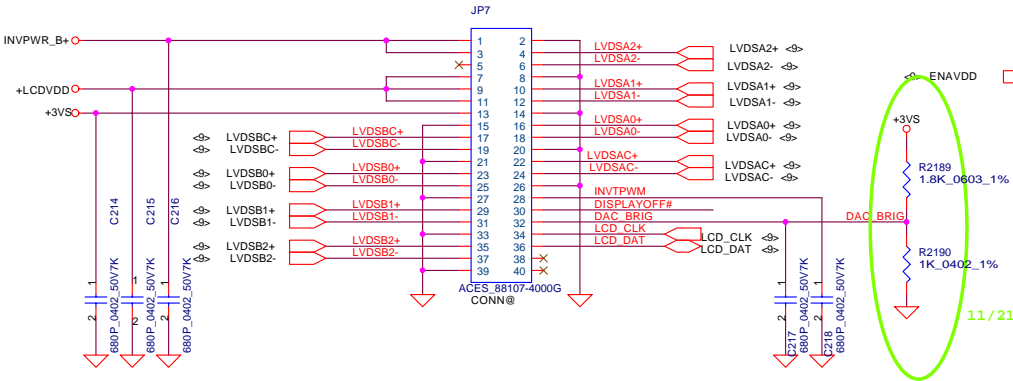
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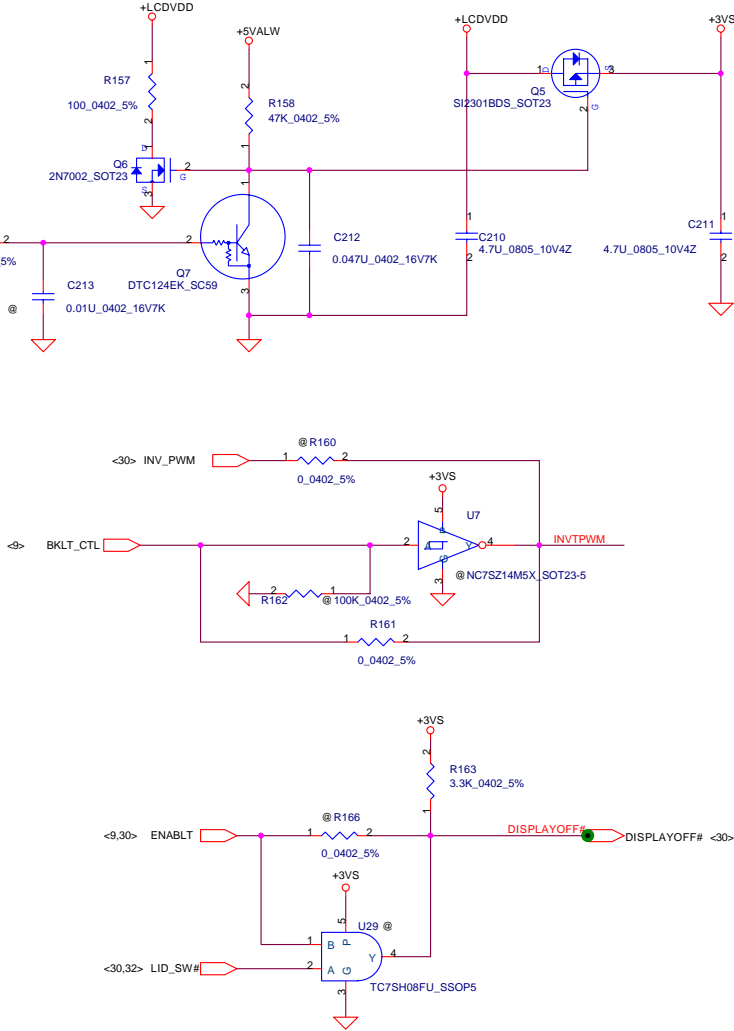
LVDS CONN



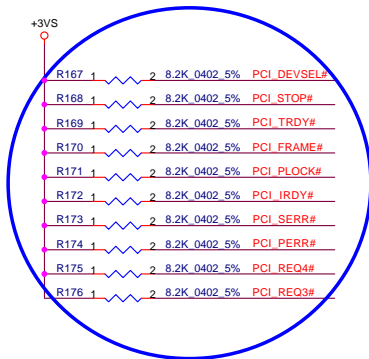
LVDS connector



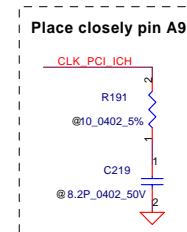
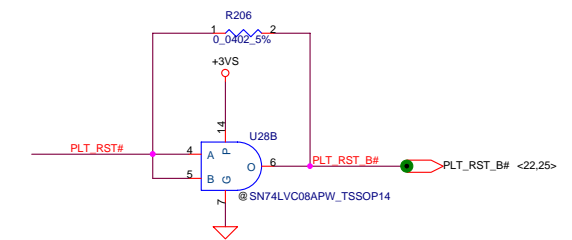
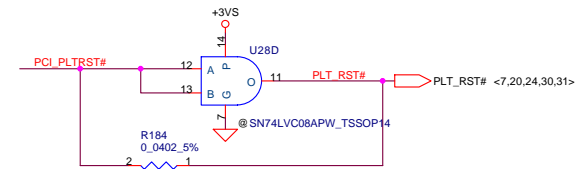
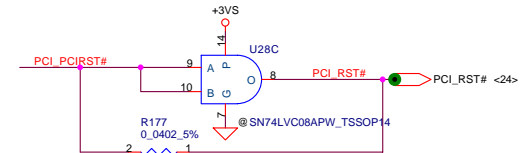
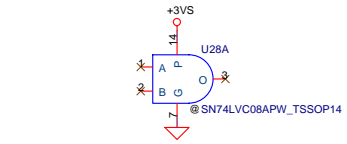
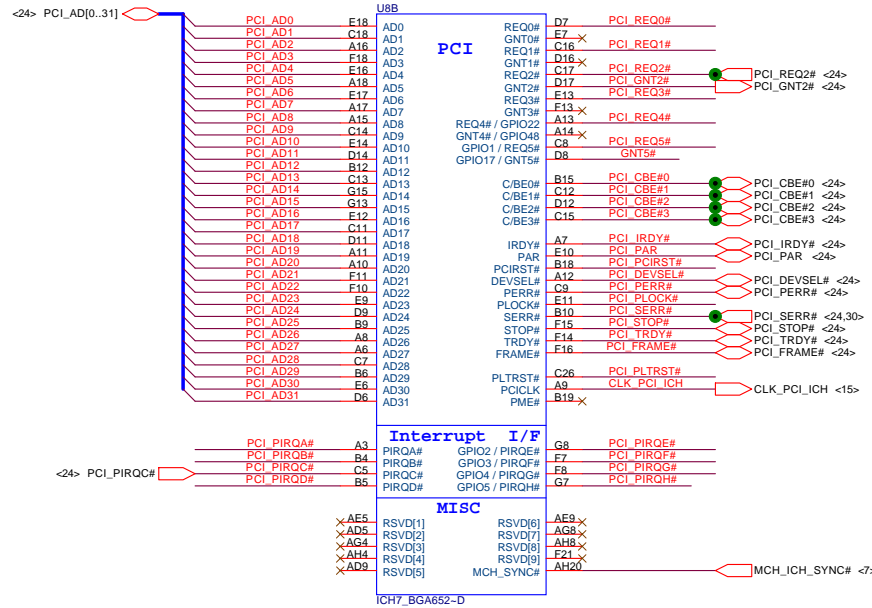
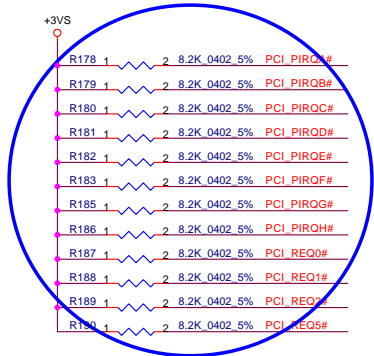
LCD/PANEL BD. CONN.



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Change to RP before SI phase



GNT5# and GNT4# have internal pull high 20K

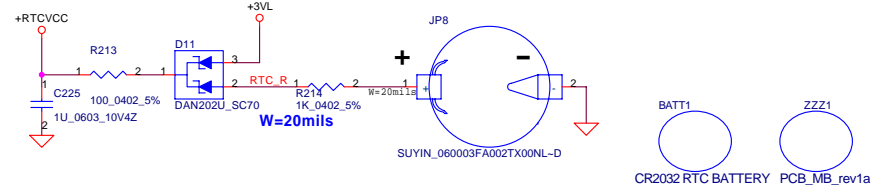
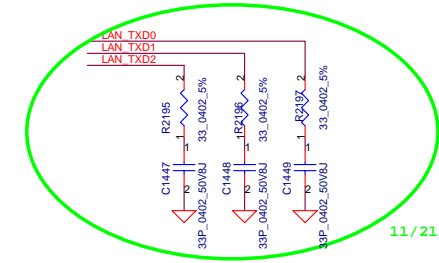
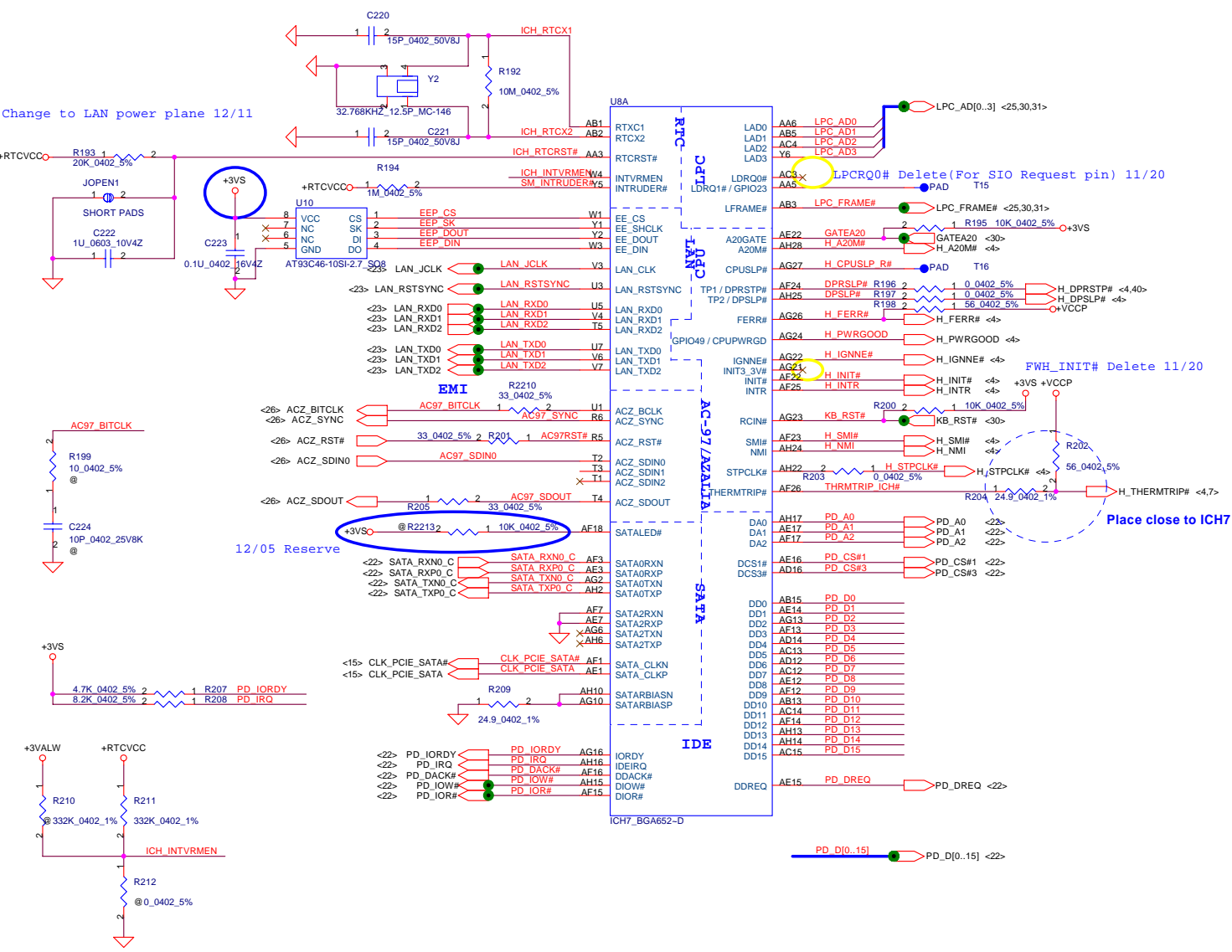
Boot BIOS destination

GNT5#	GNT4#	
0	1	SPI@ (Default)
1	0	PCI@
1	1	LPC@

The pad must be placed on PCB easily contact space for BIOS team setting.

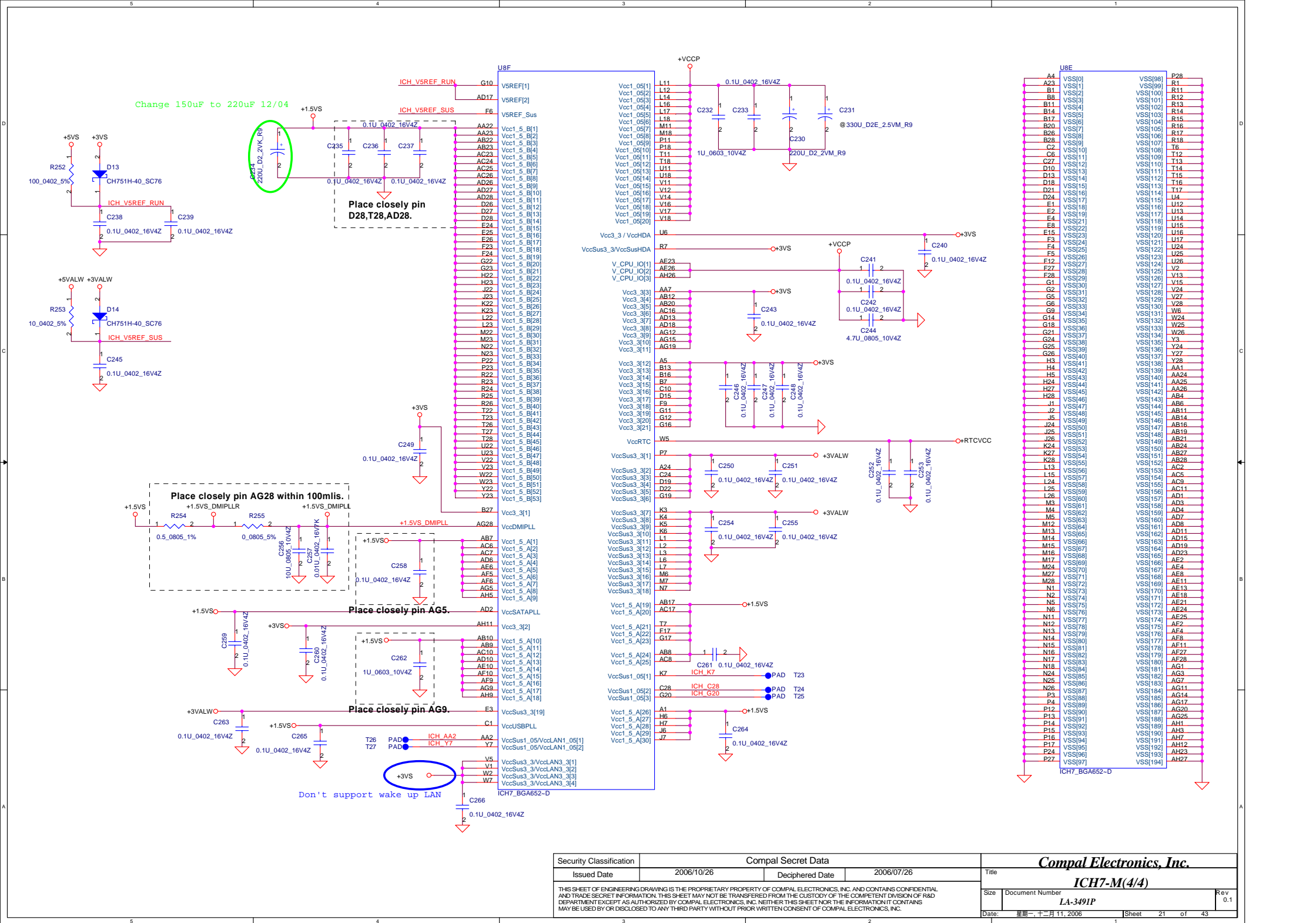
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Change to LAN power plane 12/11

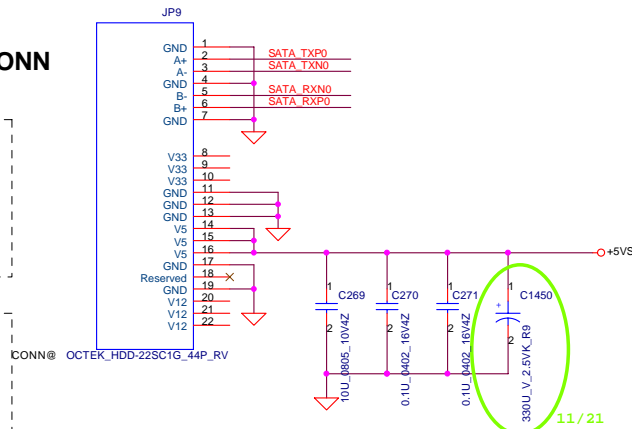
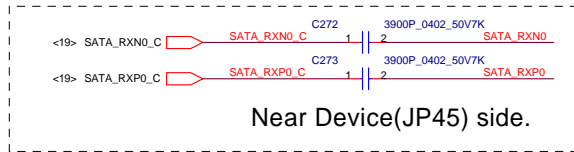
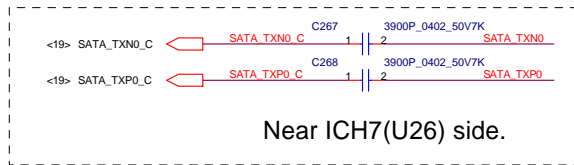


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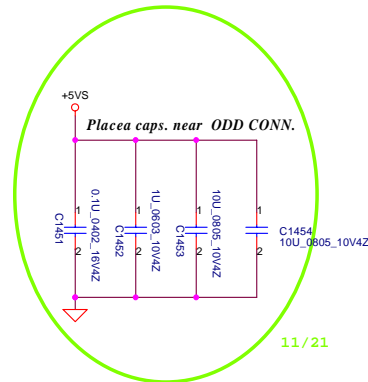
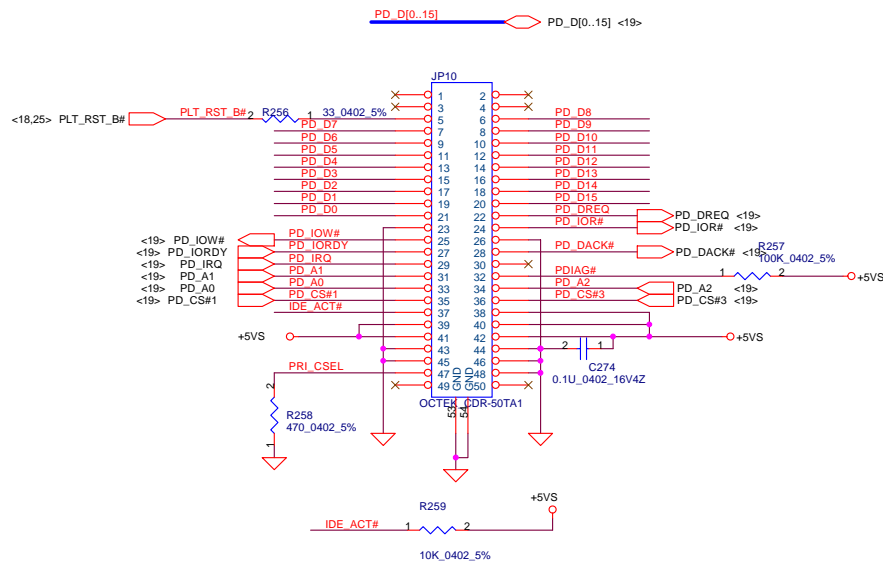




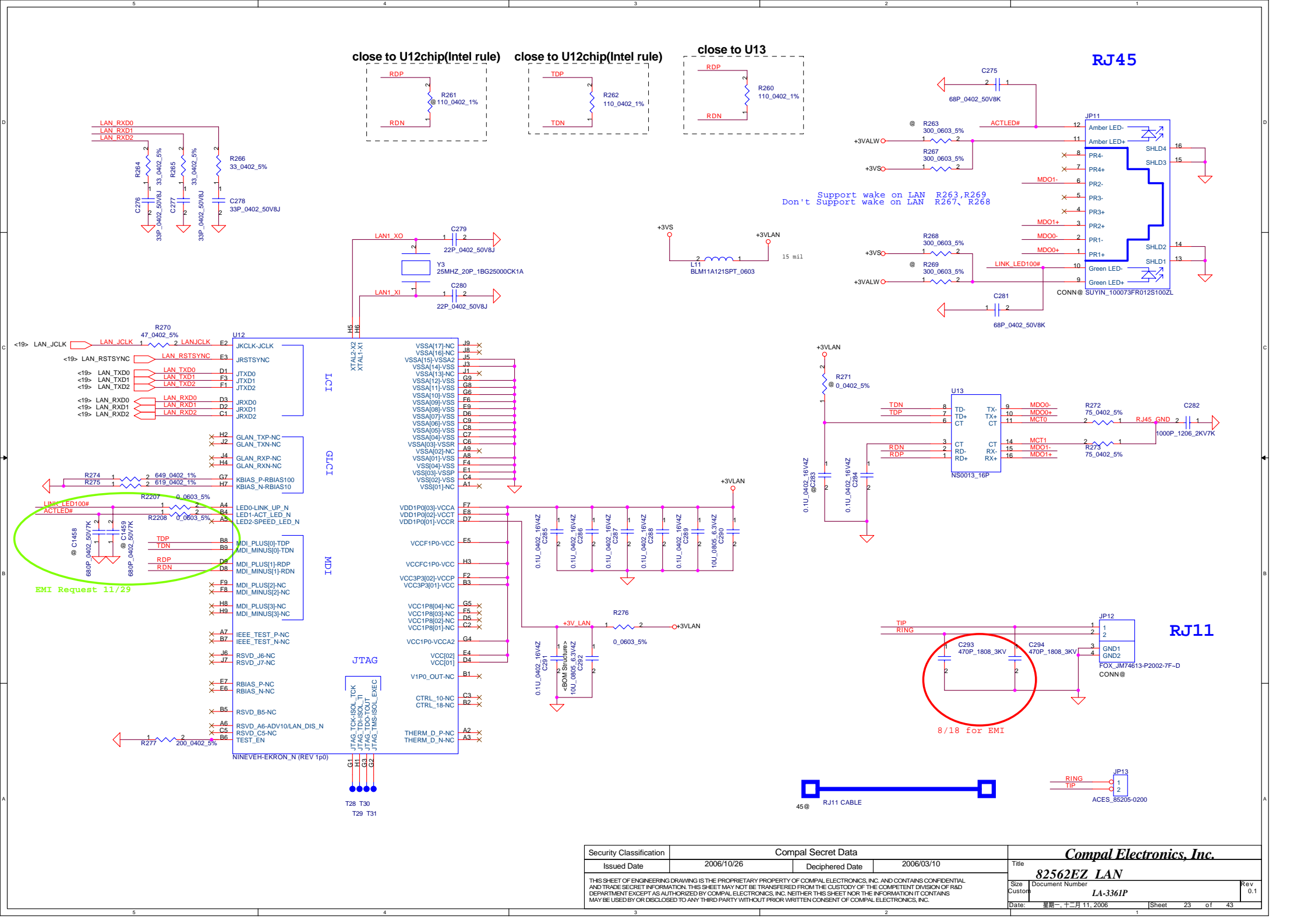
## SATA CONN



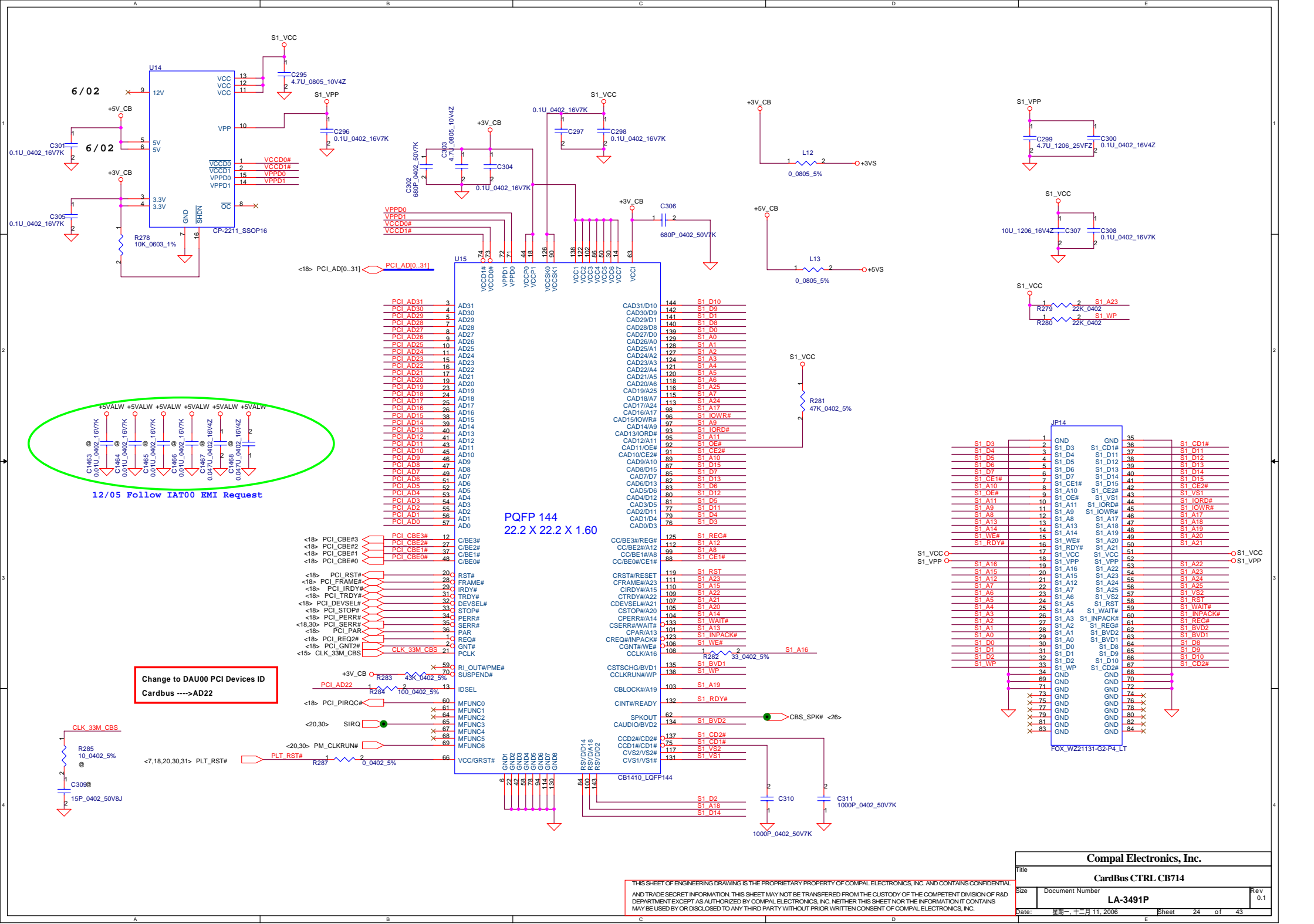
## CD-ROM Connector



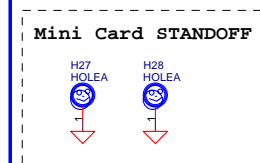
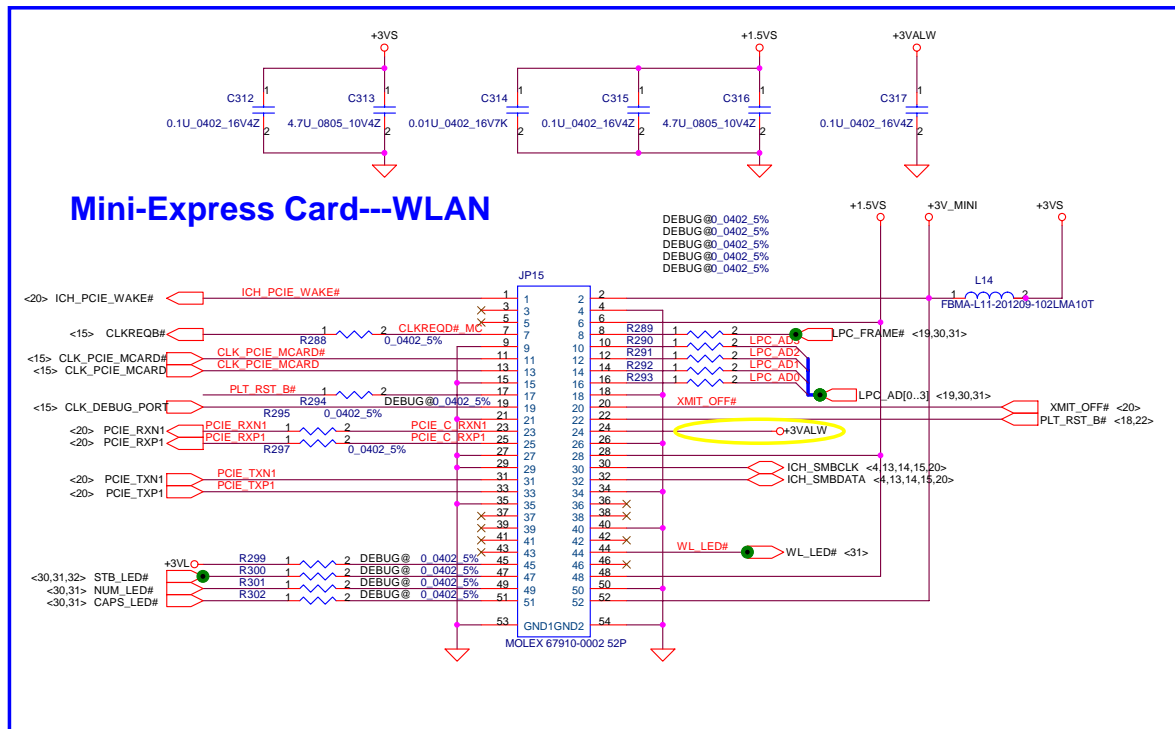
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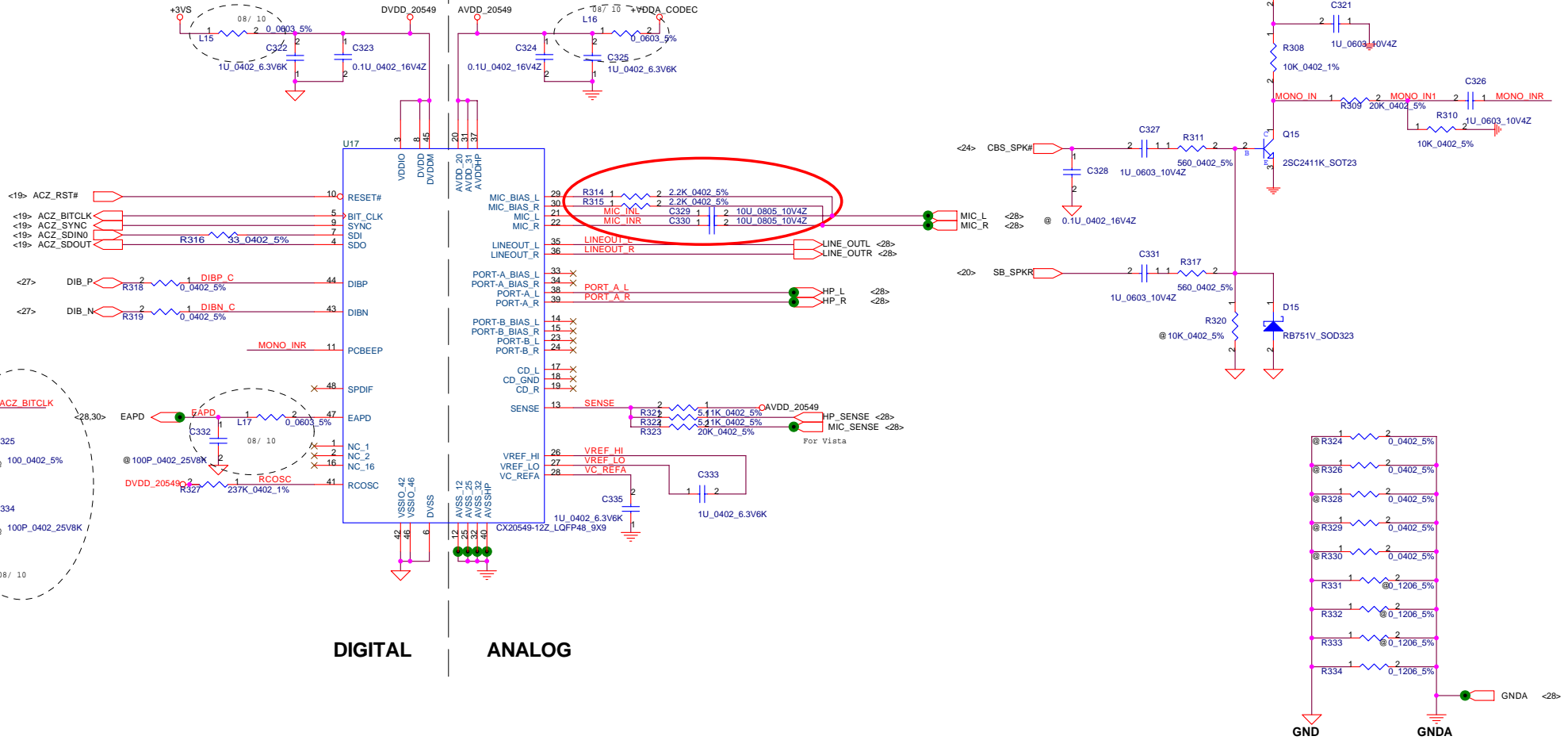
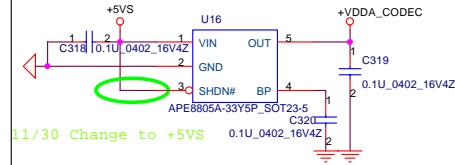


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## AUDIO CODEC

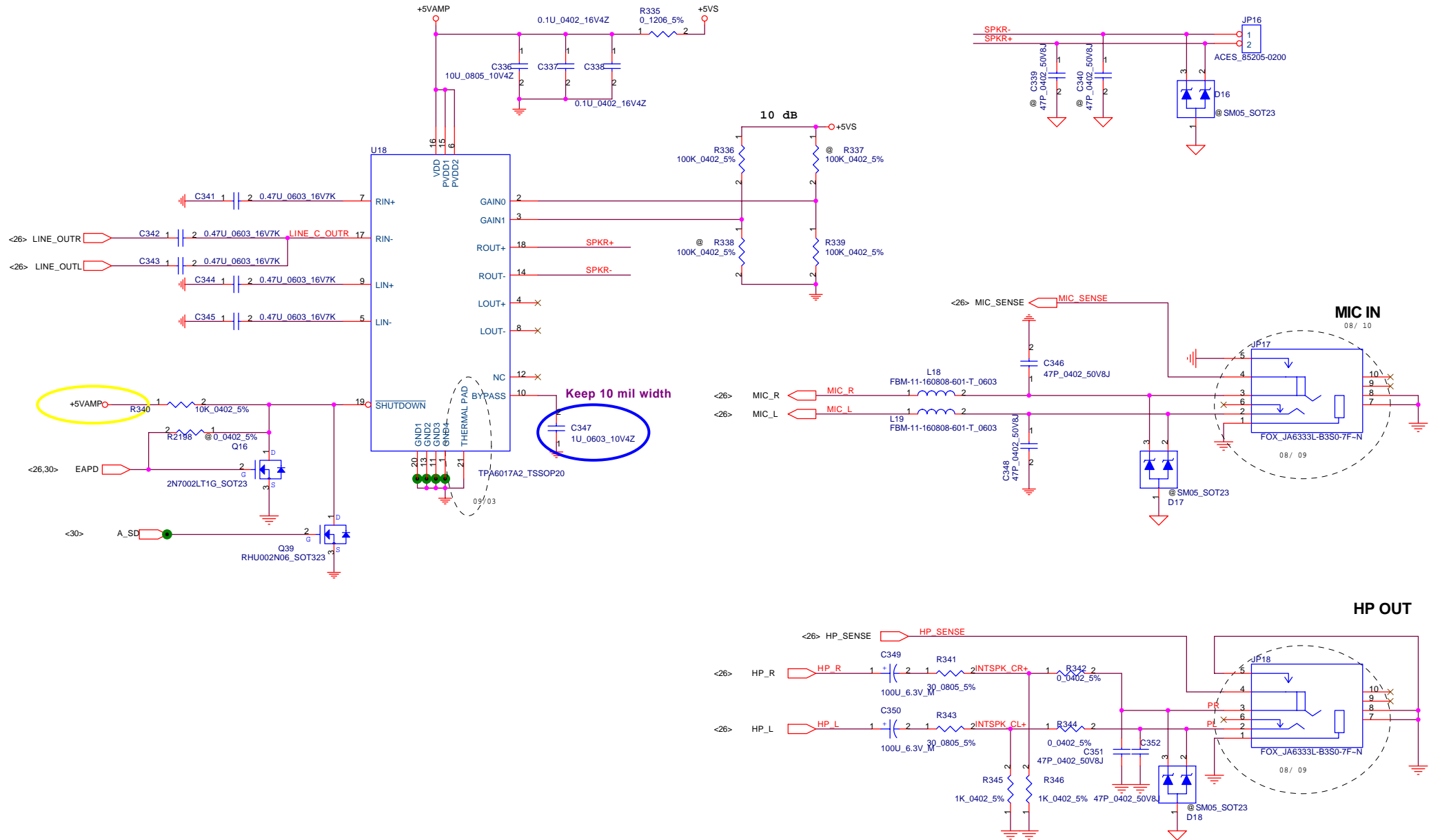
In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

## CODEC POWER



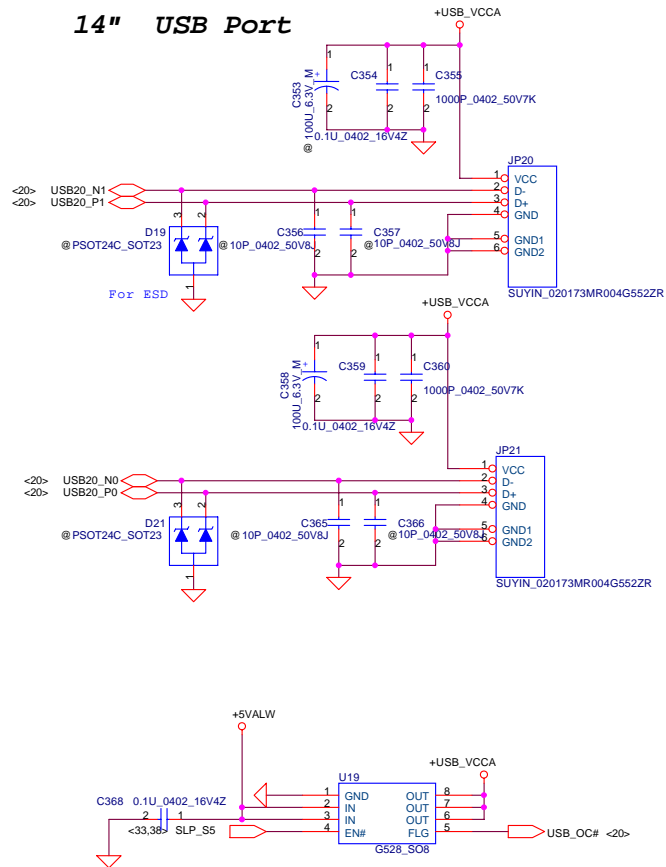
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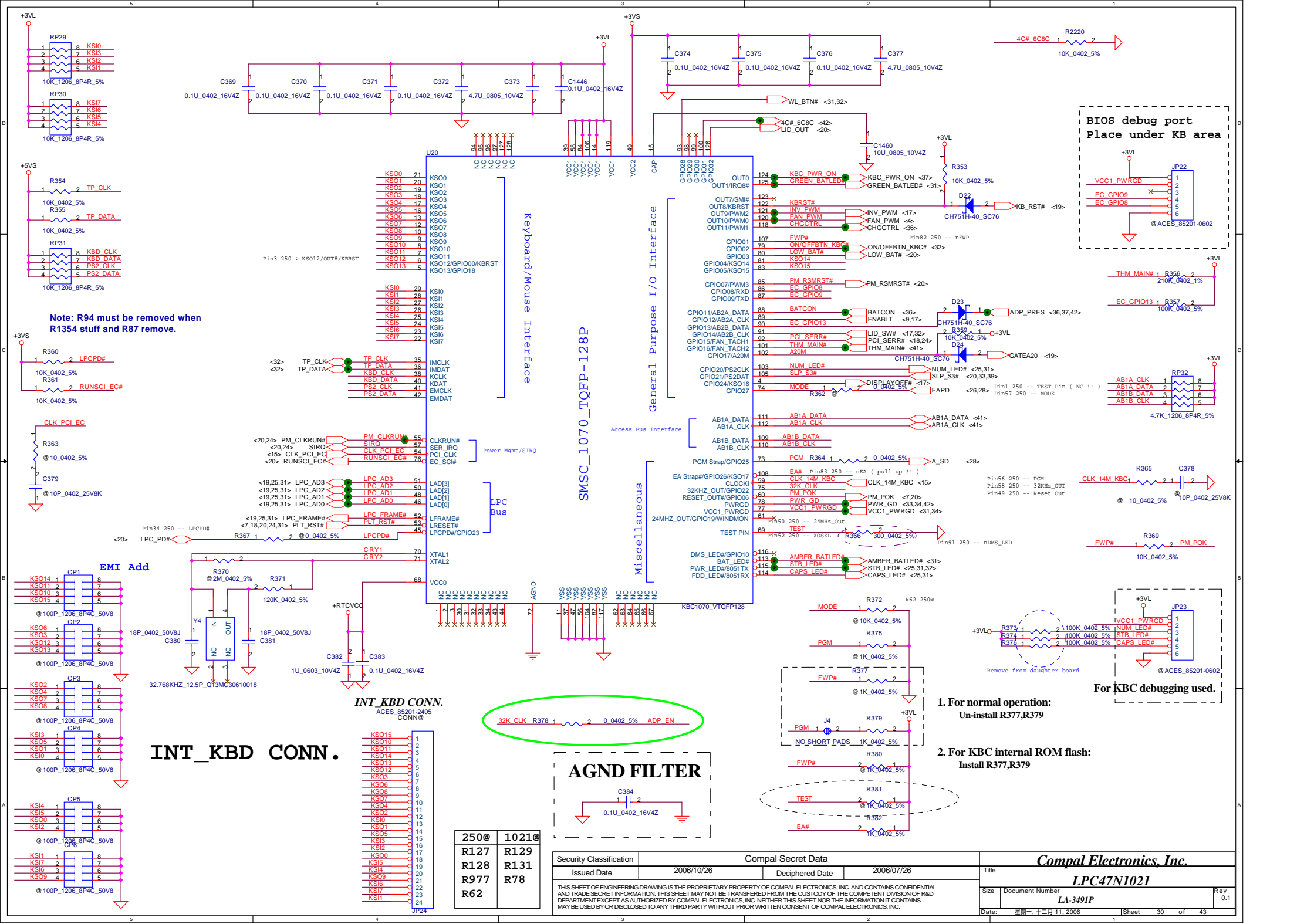


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# 14" USB Port

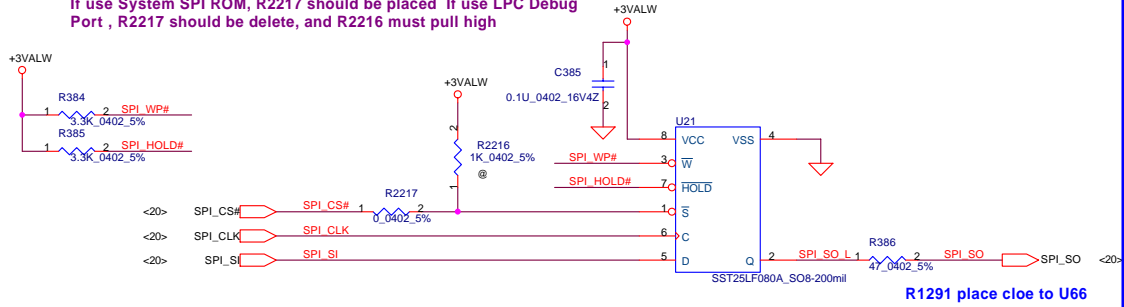


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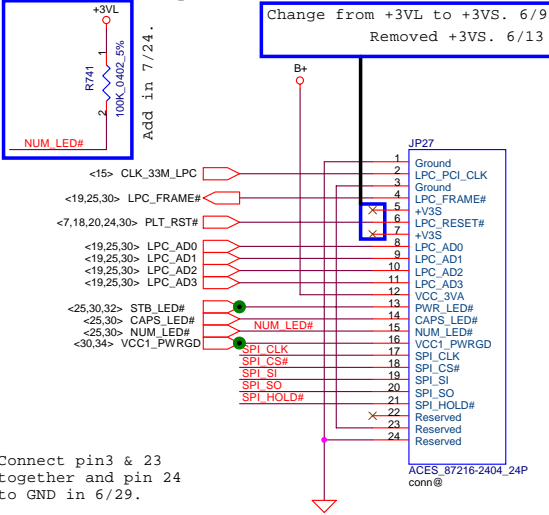


## BIOS ROM

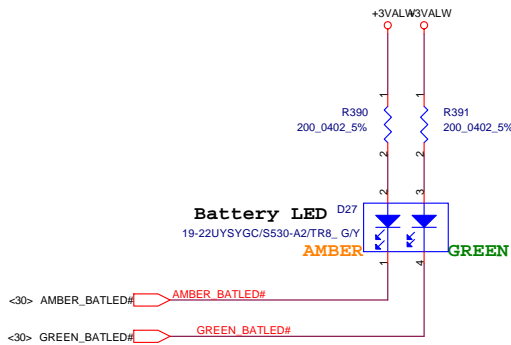
If use System SPI ROM, R2217 should be placed If use LPC Debug Port , R2217 should be delete, and R2216 must pull high



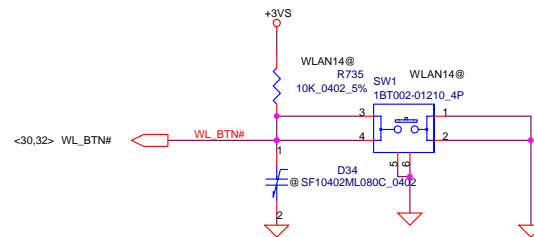
## LPC Debug Port



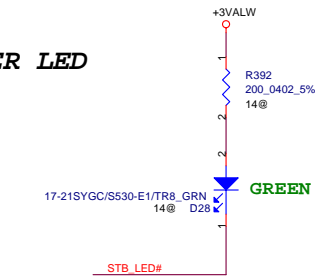
**Charge LED**



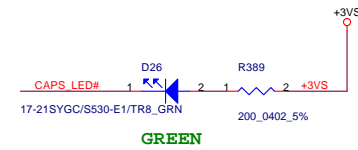
**WL ON/OFF**



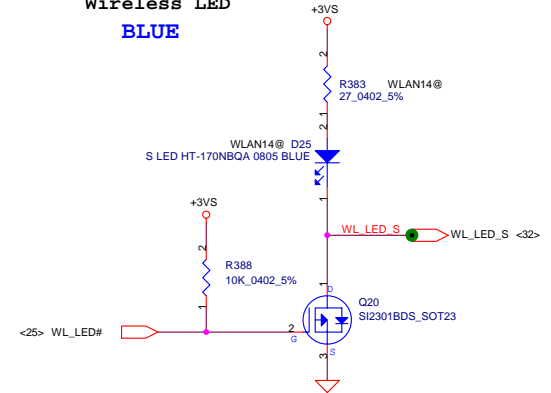
**POWER LED**



*CAP LED*



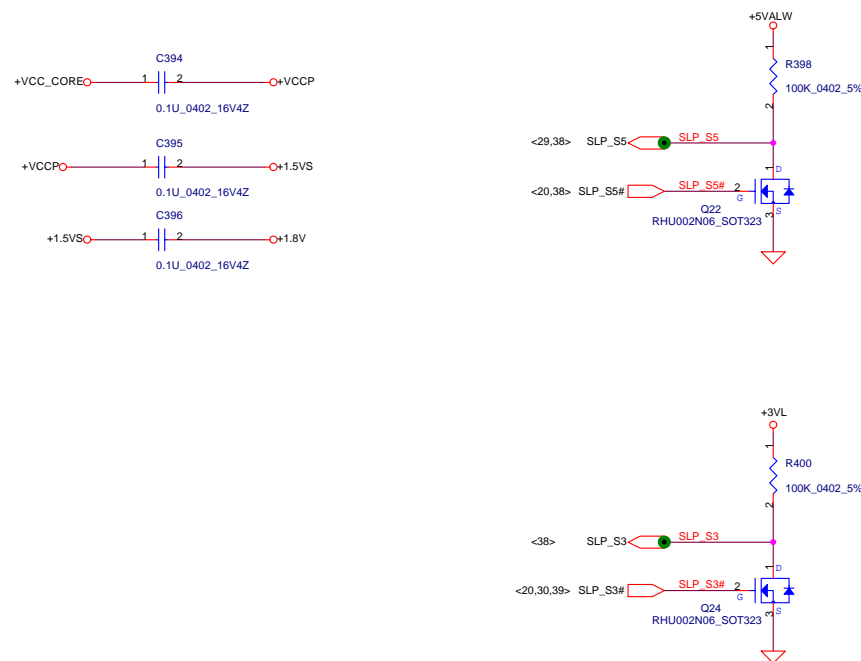
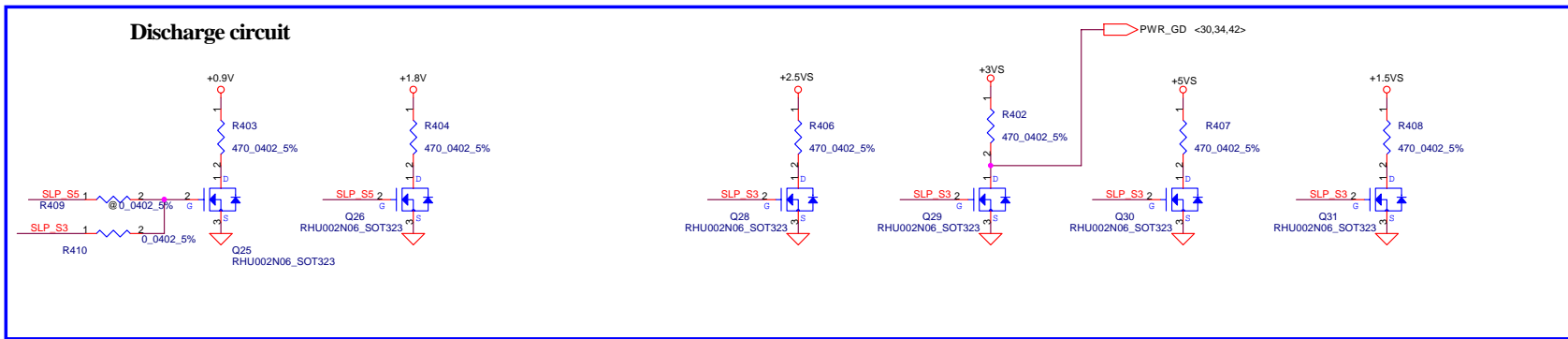
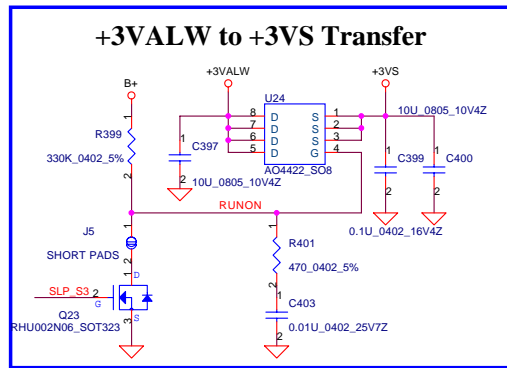
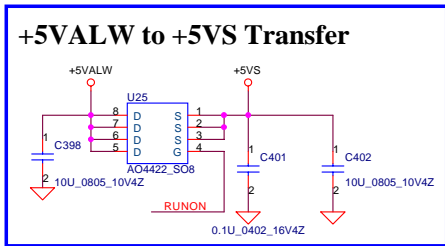
Wireless LED  
BLUE

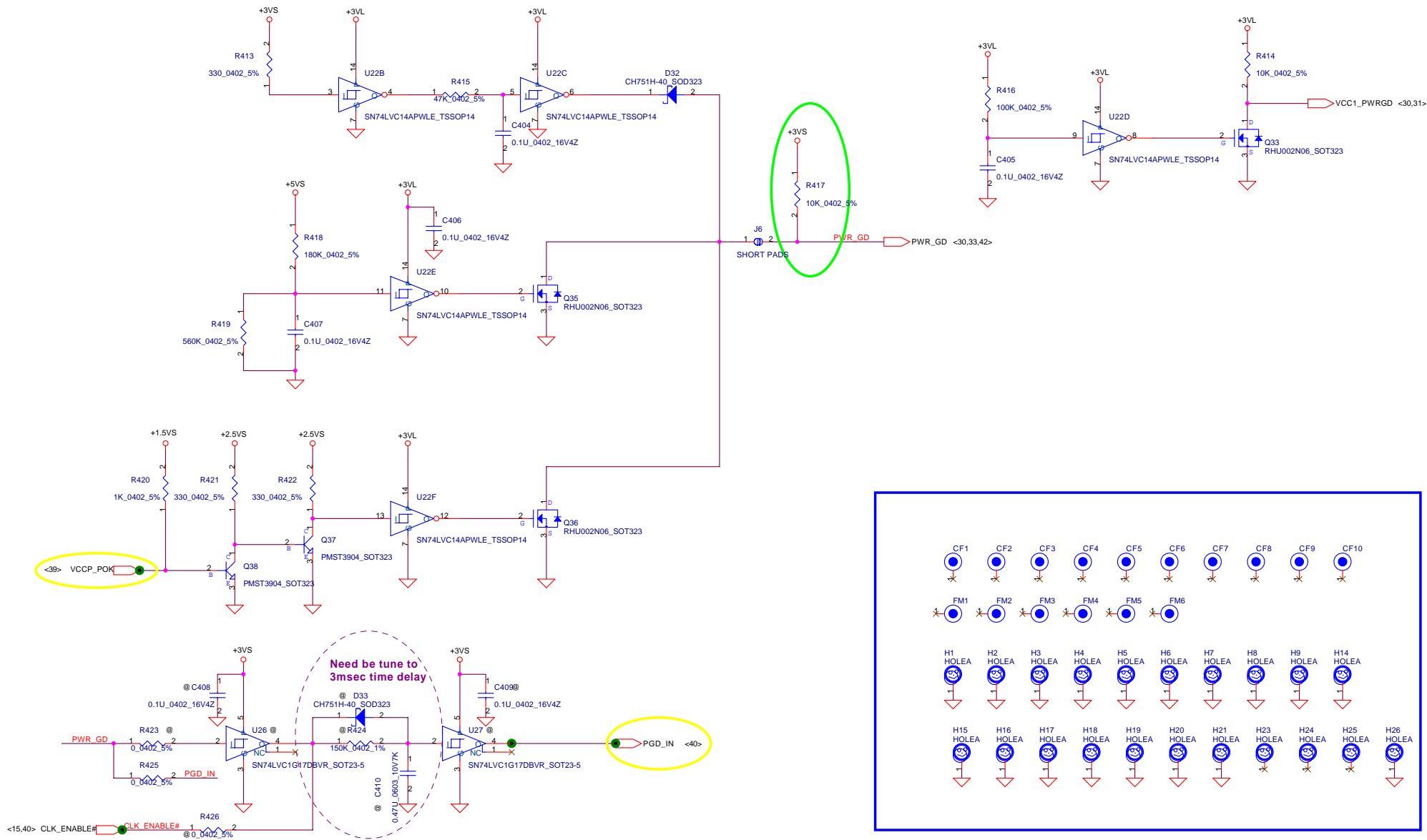


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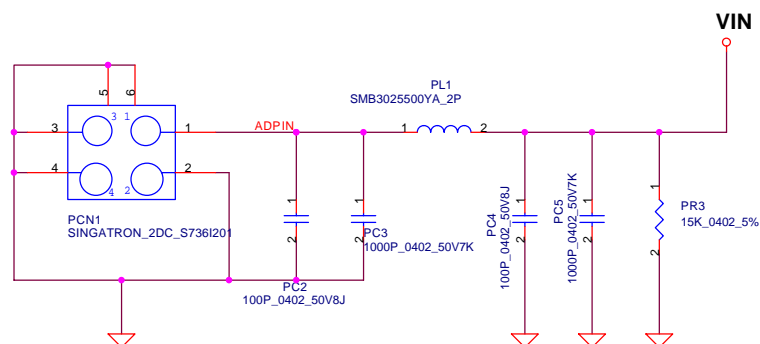




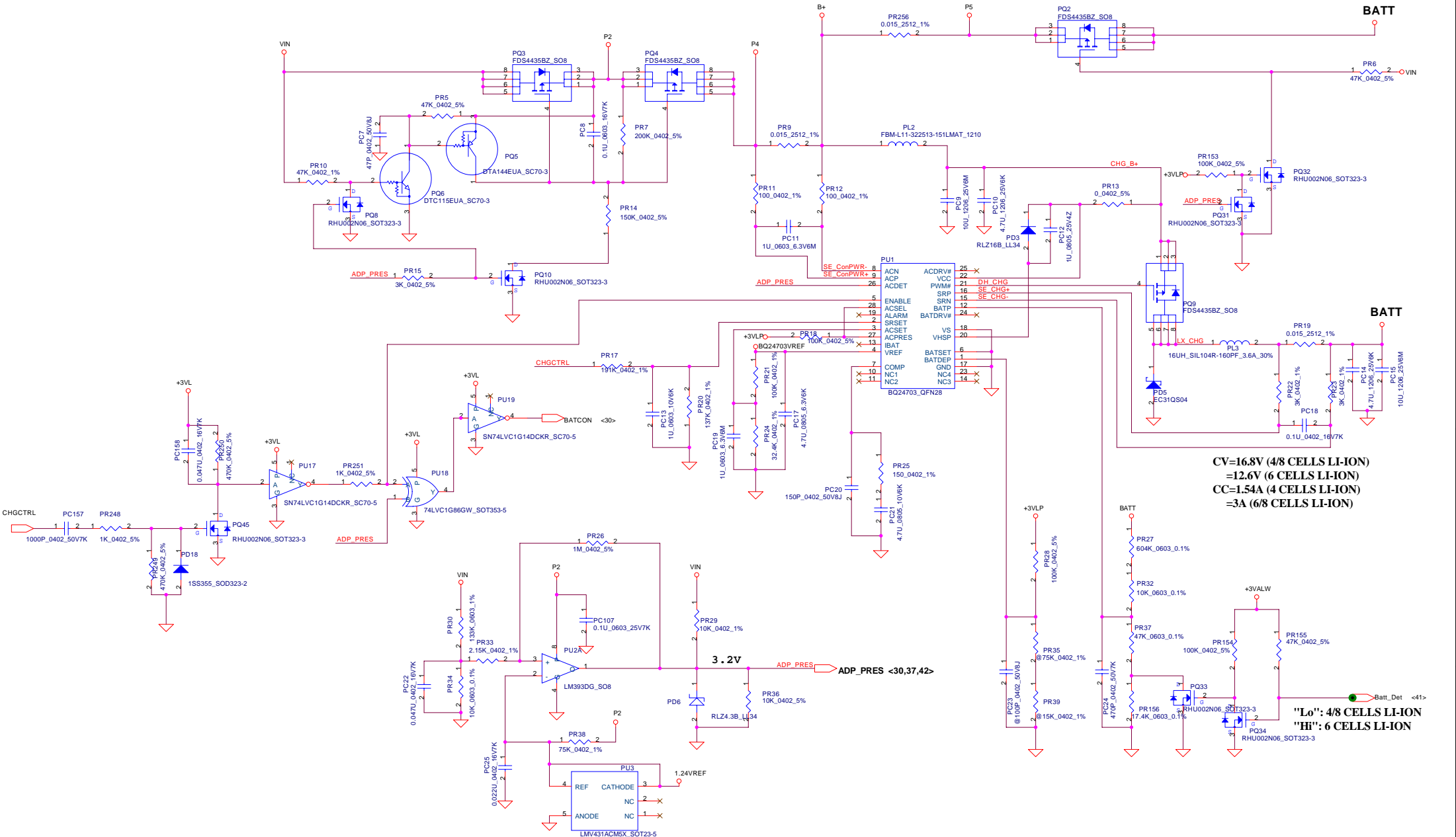




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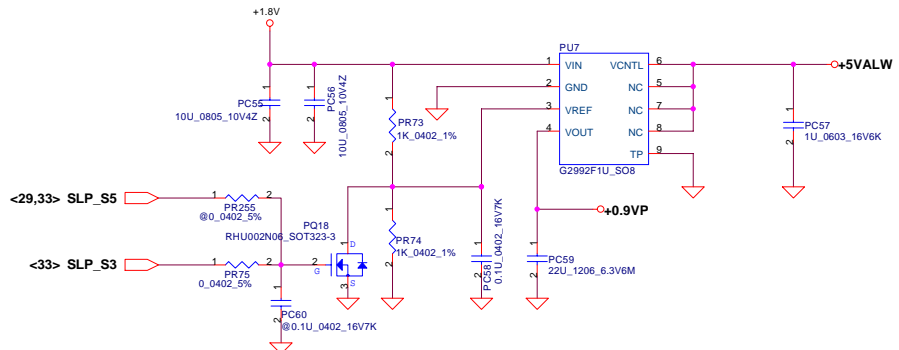
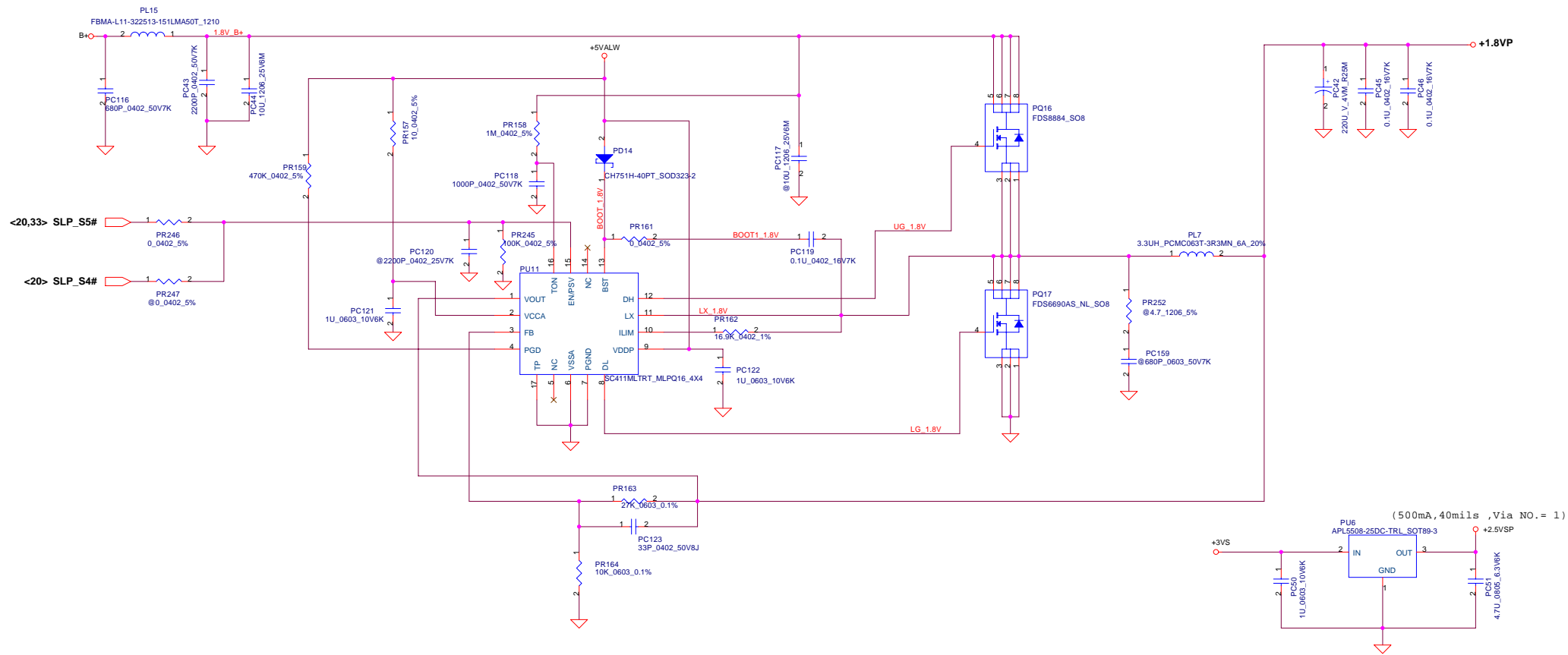


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=12.6V (6 CELLS LI-ION)  
CC=1.54A (4 CELLS LI-ION)  
=3A (6/8 CELLS LI-ION)

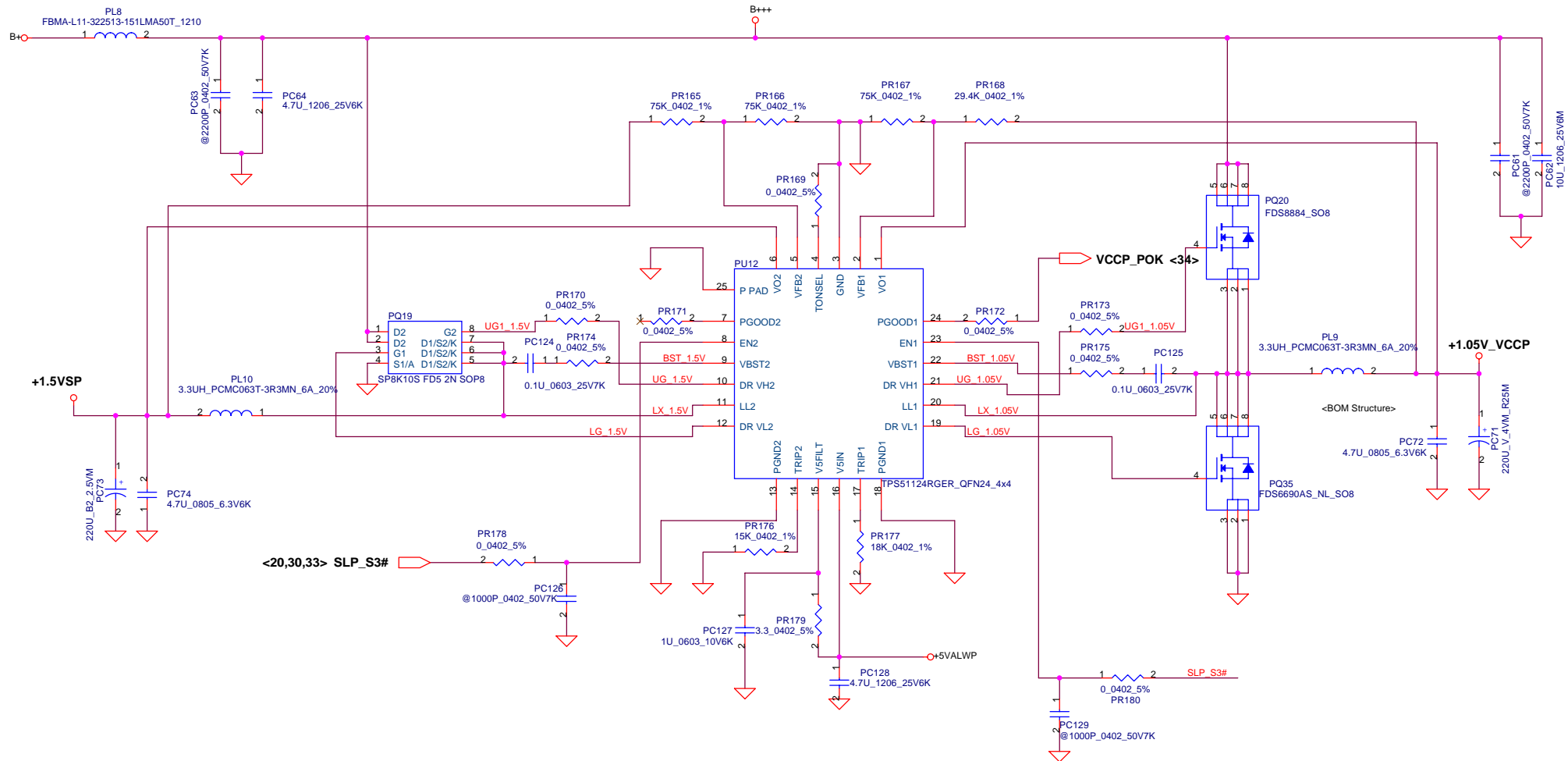
"Lo": 4/8 CELLS LI-ION  
"Hi": 6 CELLS LI-ION

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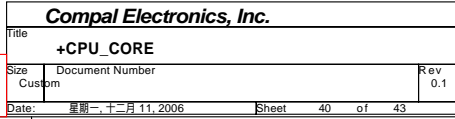




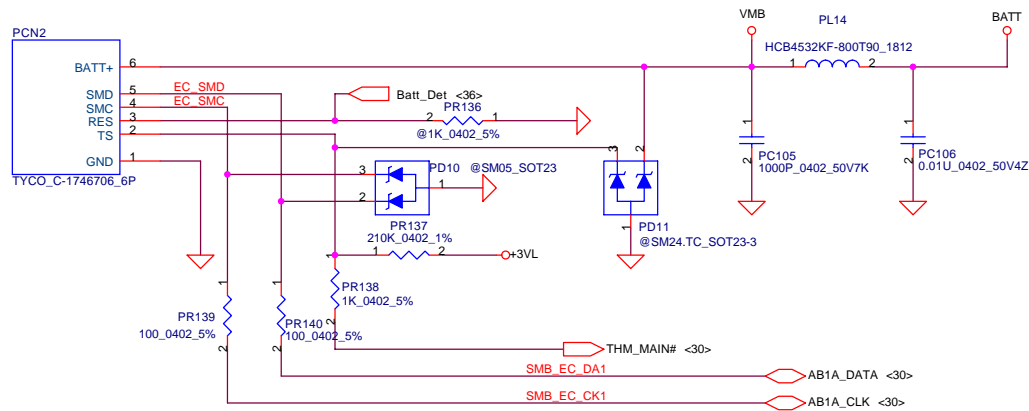
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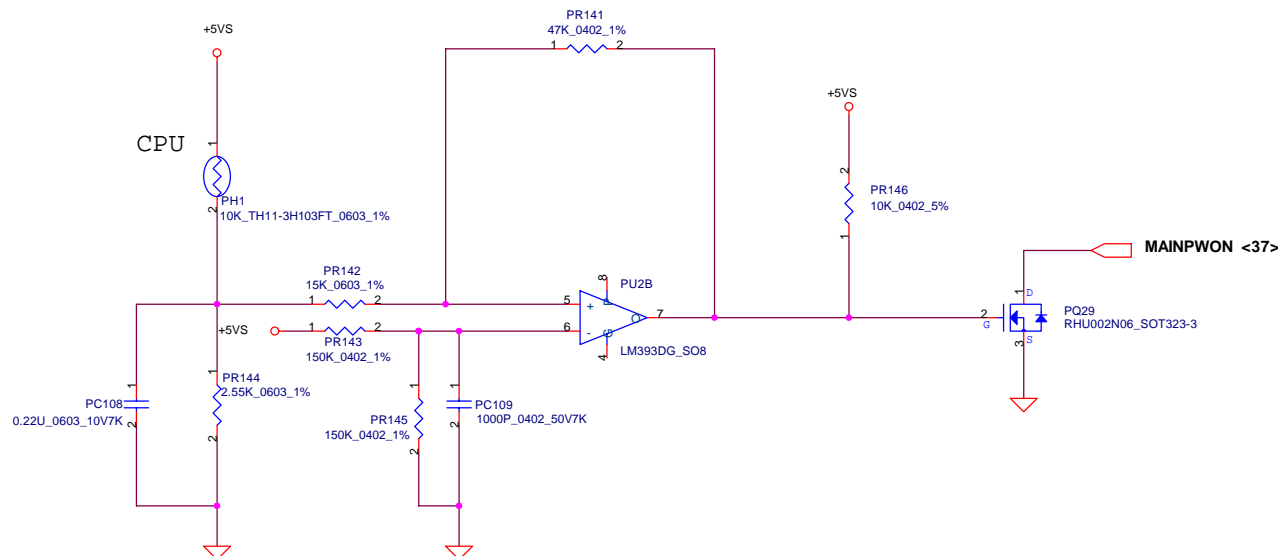
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PH1 under CPU botten side :  
CPU thermal protection at 90 +-3 degree C  
Recovery at 47 +-3 degree C



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3					
4					
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Date:	~P期一,十二月11,2006		Sheet 43 of 43